# STM303N040LSH8H

*N-Channel Enhancement Mode Field Effect Transistor*

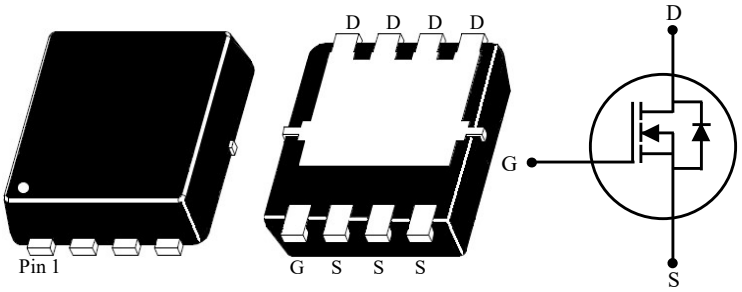
## *FEATURES*

· Low $R_{DS(on)}$

· Suffix "H" indicates Halogen-free parts, ex.STM303N040LSH8H

**PIN CONFIGURATION**

DFN3×3-8L




| | |
|---|---|
| D | Drain |
| G | Gate |
| S | Source |

## *Maximum Ratings($T_A$=25 ℃ unless otherwise noted)*

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | 30 | V |
| Gate-Source Voltage | $V_{GS}$ | ±20 | |
| Drain Current $T_C$=25℃ | $I_D$ | 48 | A |
| Drain Current $T_C$=100℃ | | 30 | |
| Pulsed Drain Current (Note 1) | $I_{DM}$ | 280 | A |
| Avalanche Current | $I_{AS}$ | 33 | A |
| Avalanche Energy (Note 2) | $E_{AS}$ | 54.5 | mJ |
| Power Dissipation $T_C$=25℃ | $P_D$ | 15.6 | W |
| Thermal Resistance from Junction to Ambient (Note 3) | $R_{\theta JA}$ | 50 | ℃/W |
| Thermal Resistance from Junction to Case | $R_{\theta JC}$ | 8 | ℃/W |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{stg}$ | - 55 to + 150 | ℃ |

Note:

1. The data tested by pulsed, pulse width ≦100μs, duty cycle ≦2%, Reptitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150°C

2. Limited by $T_{J(MAX)}$, starting $T_J$=25℃, L=0.1mH, $R_g$=25Ω, $I_{AS}$=33A, $V_{GS}$=10V.

3. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch$^2$ copper plate in still air.

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*N-Channel Enhancement Mode Field Effect Transistor*

## *Electrical Characteristics($T_A$=25 ℃ unless otherwise specified)*

| Parameter | Conditions | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Drain-Source Breakdown Voltage | $I_D$=250μA | $V_{(BR)DSS}$ | 30 | - | - | V |
| Gate Threshold Voltage | $V_{DS}$=$V_{GS}$, $I_D$=250μA | $V_{GS(th)}$ | 1.2 | - | 2.5 | V |
| Zero Gate Voltage Drain Current | $V_{DS}$=30V | $I_{DSS}$ | - | - | 1 | μA |
| Gate Leakage Current | $V_{GS}$=±20V | $I_{GSS}$ | - | - | ±100 | nA |
| Drain-Source On-Resistance | $V_{GS}$=10V, $I_D$=24A | $R_{DS(on)}$ | - | 3.2 | 4.0 | mΩ |
| | $V_{GS}$=4.5V, $I_D$=12A | | - | - | 5.5 | |
| Forward Transconductance | $V_{DS}$=5V, $I_D$=24A | $g_{FS}$ | - | 27 | - | S |
| **Dynamic** | | | | | | |
| Gate Resistance | $V_{DS}$=0V, $V_{GS}$=0V, f=1MHz | $R_g$ | - | 1 | - | Ω |
| Total Gate Charge | $V_{DS}$=15V, $V_{GS}$=4.5V, $I_D$=24A | $Q_g$ | - | 26.0 | - | nC |
| | $V_{DS}$=15V, $V_{GS}$=10V, $I_D$=24A | | - | 53.0 | - | |
| Gate-Source Charge | | $Q_{gs}$ | - | 8.5 | - | |
| Gate-Drain Charge | | $Q_{gd}$ | - | 13.0 | - | |
| Input Capacitance | $V_{DS}$=15V, $V_{GS}$=0V, f=1MHz | $C_{iss}$ | - | 2300 | - | pF |
| Output Capacitance | | $C_{oss}$ | - | 278 | - | |
| Reverse Transfer Capacitance | | $C_{rss}$ | - | 229 | - | |
| Turn on Delay Time | $V_{DS}$=15V, $I_D$=24A<br>$V_{GS}$=10V, $R_g$=3.3Ω | $t_{d(on)}$ | - | 18 | - | ns |
| Turn on Rise Time | | $t_r$ | - | 54 | - | |
| Turn off Delay Time | | $t_{d(off)}$ | - | 18 | - | |
| Turn off Fall Time | | $t_f$ | - | 7 | - | |
| **Drain-Source Body Diode** | | | | | | |
| Diode Forward Voltage | $V_{GS}$=0V, $I_S$=1A | $V_{SD}$ | - | - | 1.2 | V |
| Diode Continuous Forward Current | - | $I_S$ | - | - | 48 | A |
| Diode Pulse Current | | $I_{SM}$ | - | - | 280 | A |
| Reverse Recovery Time | $I_S$=24A, di/dt=100A/μs | $t_{rr}$ | - | 15.5 | - | ns |
| Reverse Recovery Charge | | $Q_{rr}$ | - | 6.4 | - | nC |

## *RATINGS AND CHARACTERISTIC CURVES*

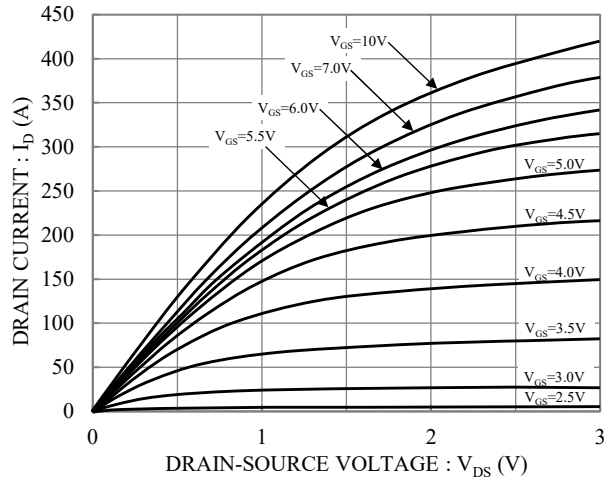



**Fig.1 Typical Output Characteristics**

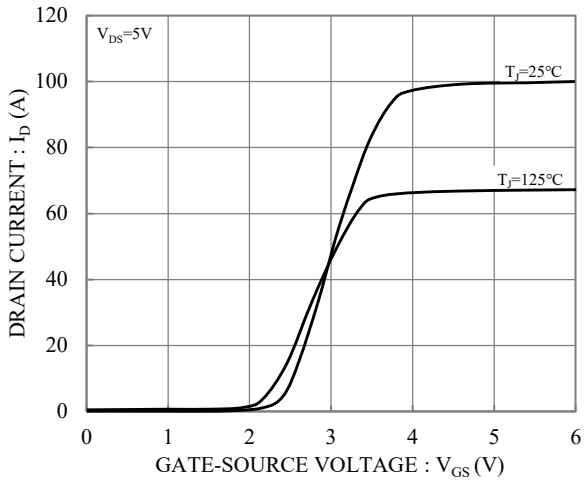



**Fig.2 Typical Transfer Characteristics**

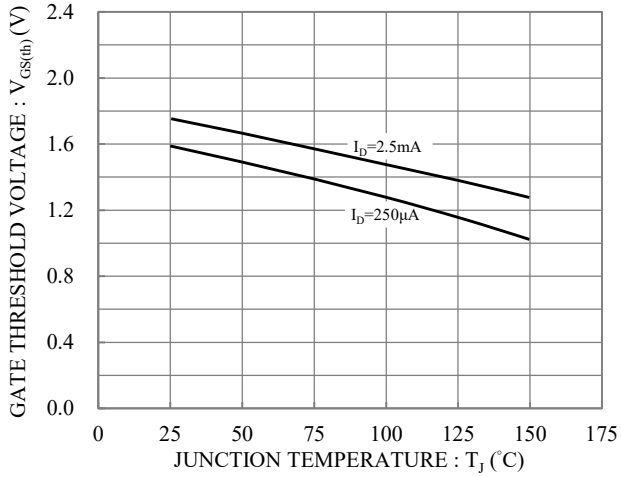



**Fig.3 Gate Threshold Voltage vs. Junction Temperature**

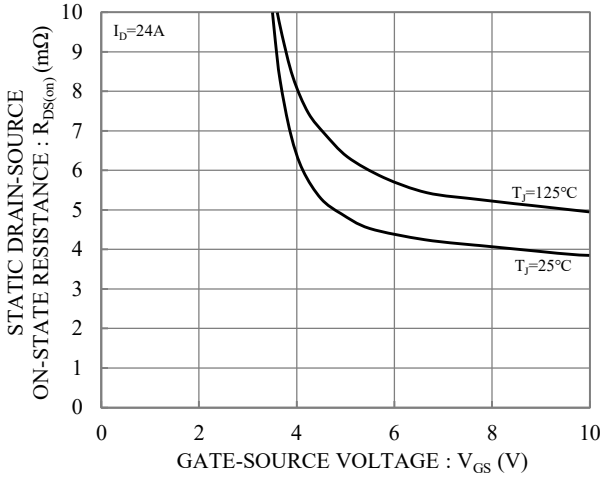



**Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage**

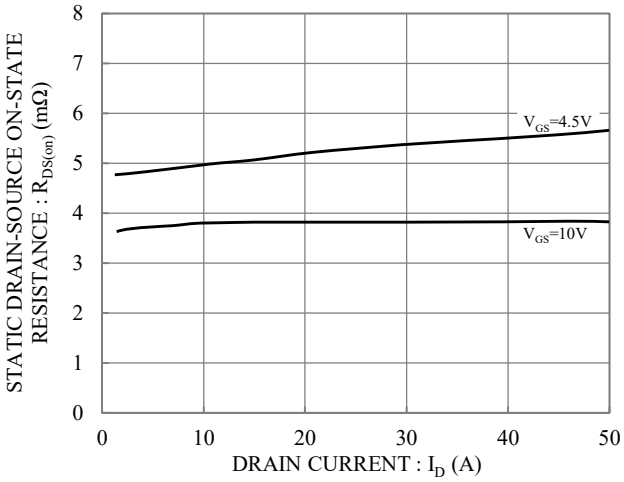



**Fig.5 Static Drain-Source On-State Resistance vs. Drain Current**

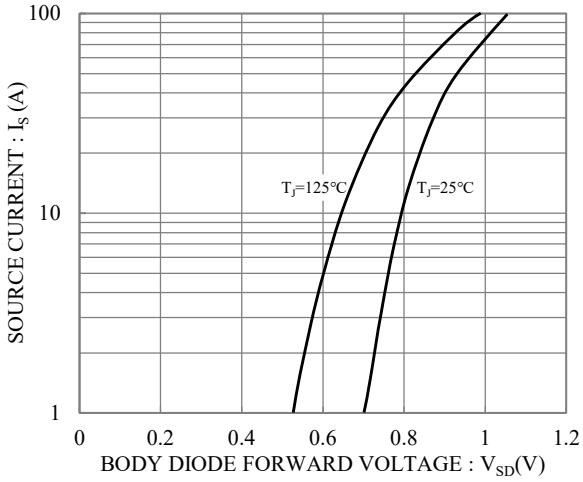



**Fig.6 Body Diode Forward Voltage vs. Source Current**

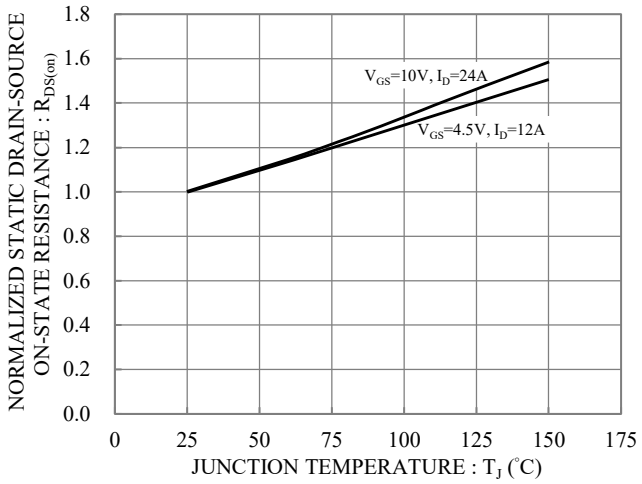



**Fig.7 Drain-Source On-State Resistance vs. Junction Tempearture**

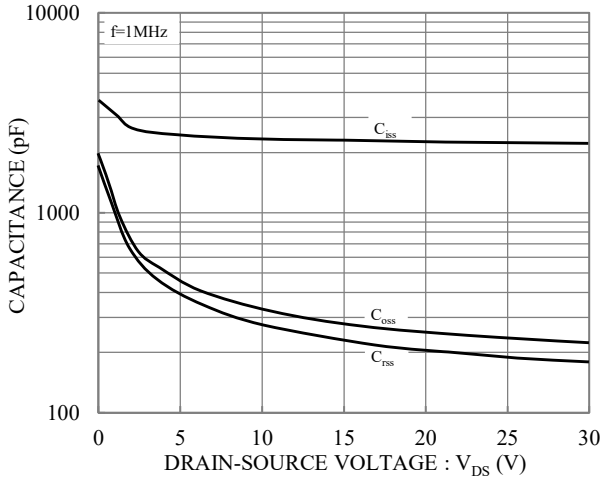



**Fig.8 Capacitance vs. Drain-Source Voltage**

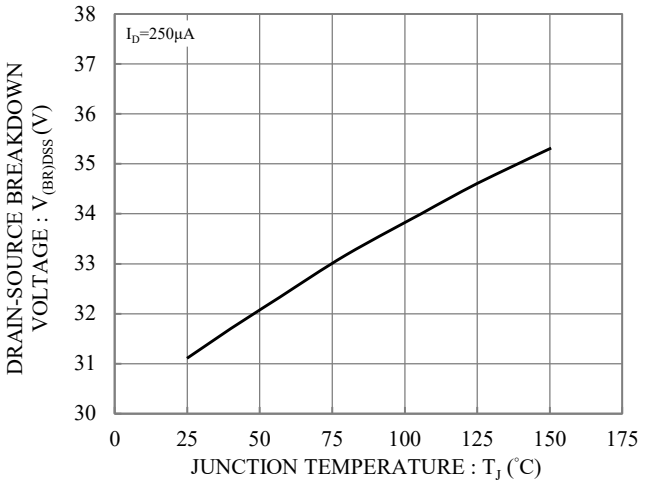



**Fig.9 Breakdown Voltage vs. Junction Temperature**

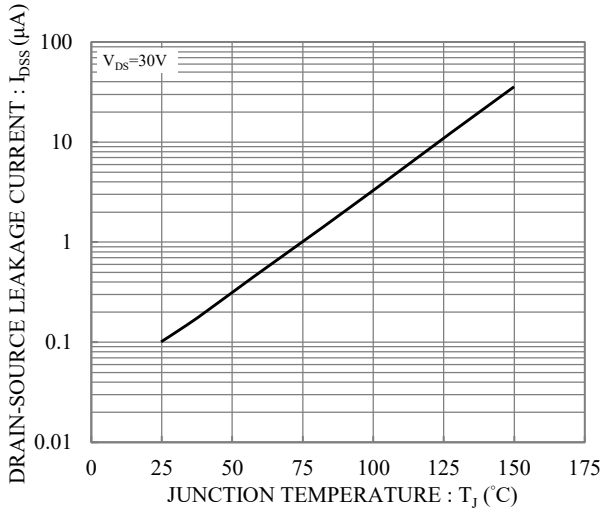



**Fig.10 Drain-Source Leakge Current vs. Junction Temperature**

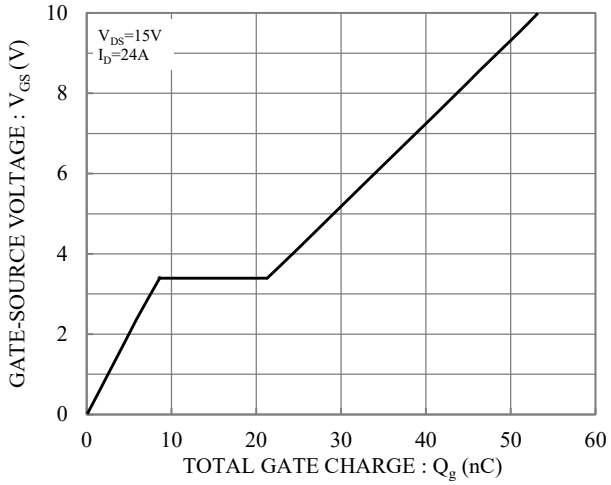



**Fig.11 Gate Charge Characteristics**

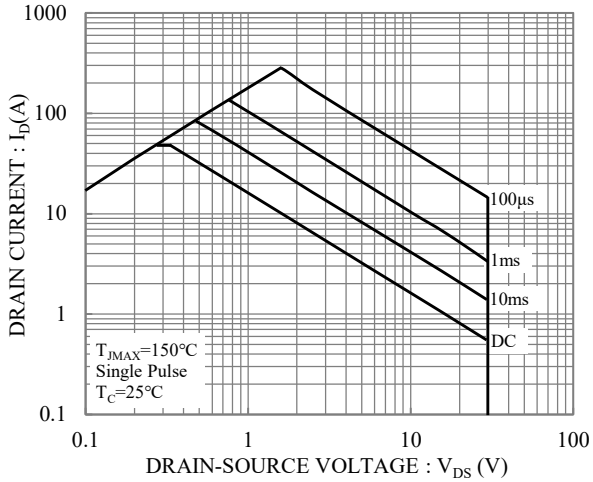



**Fig.12 Safe Operation Area**

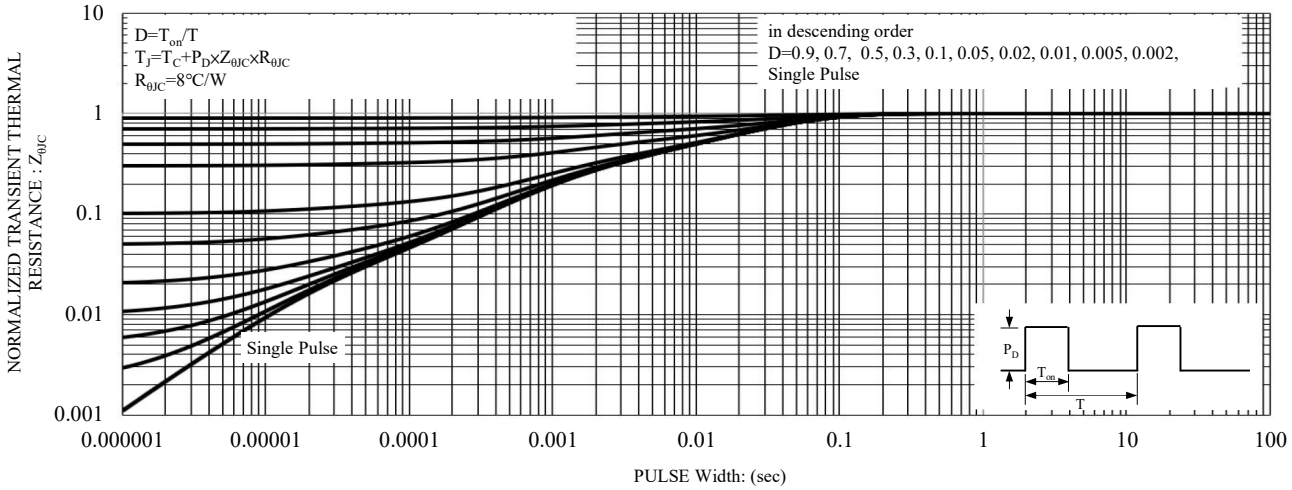



**Fig.13 Maximum Transient Thermal Impedance**

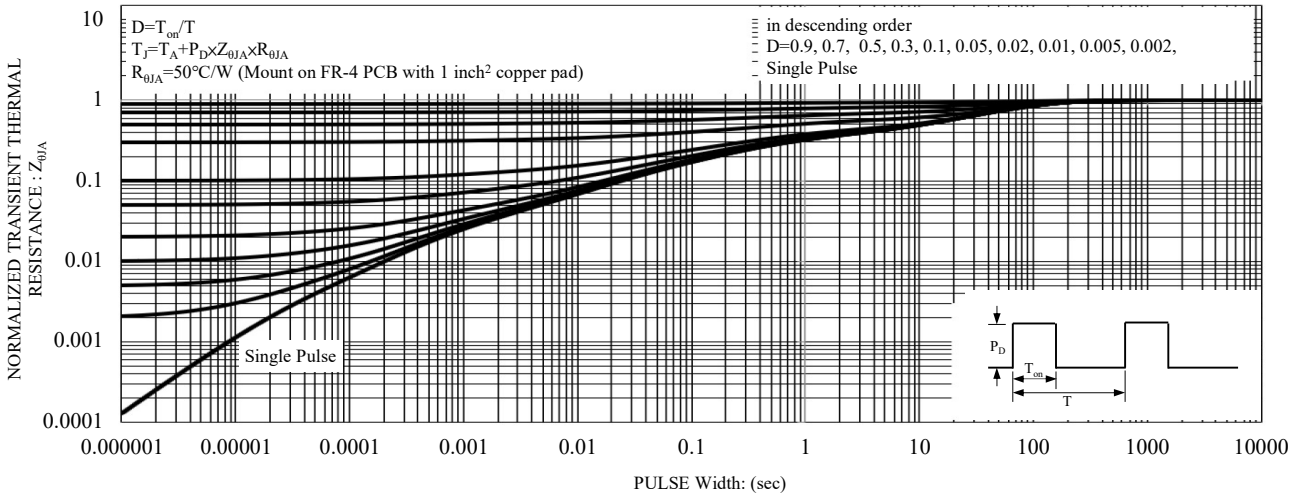
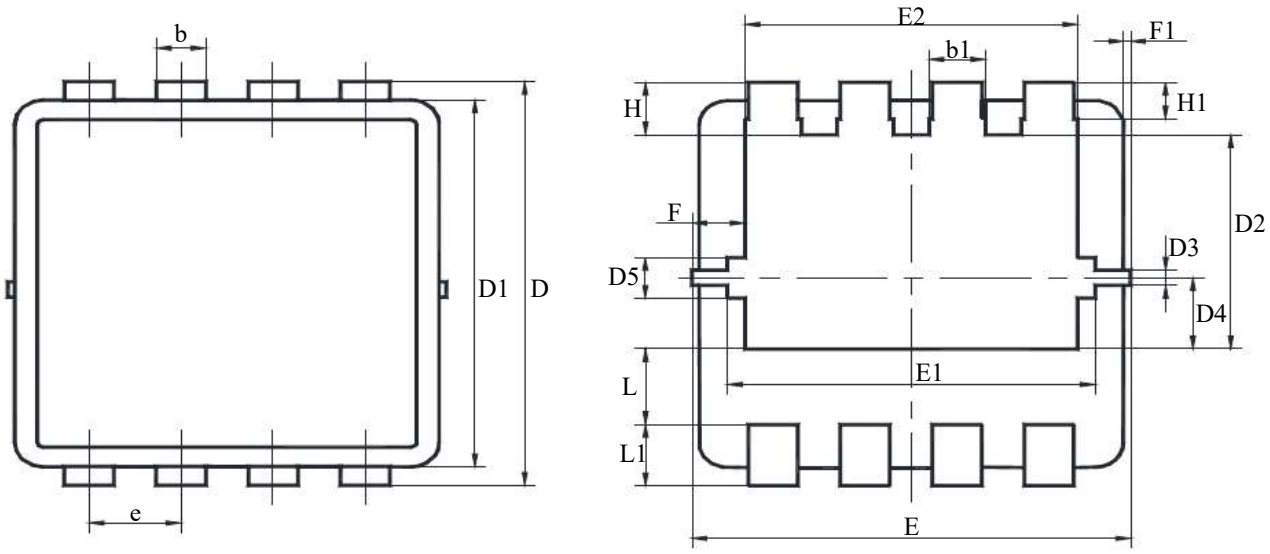



**Fig.14 Maximum Transient Thermal Impedance**

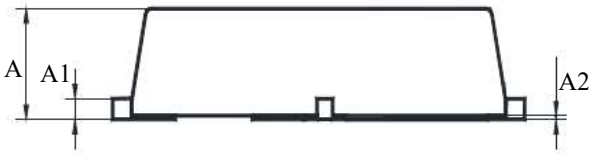
## *PACKAGE DIMENSION*

### DFN3×3-8L




Top View

Bottom View




Side View

| Symbol | Millimeters | | Inches | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| **A** | 0.700 | 0.900 | 0.028 | 0.035 |
| **A1** | 0.100 | 0.250 | 0.004 | 0.010 |
| **A2** | 0.000 | 0.050 | 0.000 | 0.002 |
| **b** | 0.240 | 0.350 | 0.009 | 0.014 |
| **b1** | 0.300 | 0.500 | 0.012 | 0.020 |
| **D** | 3.100 | 3.300 | 0.122 | 0.130 |
| **D1** | 2.900 | 3.100 | 0.114 | 0.122 |
| **D2** | 1.650 | 1.850 | 0.065 | 0.073 |
| **D3** | 0.150 | 0.250 | 0.006 | 0.010 |
| **D4** | 0.480 | 0.680 | 0.019 | 0.027 |
| **D5** | 0.230 | 0.430 | 0.009 | 0.017 |
| **E** | 3.000 | 3.200 | 0.118 | 0.126 |
| **E1** | 2.500 | 2.700 | 0.098 | 0.106 |
| **E2** | 2.400 | 2.600 | 0.094 | 0.102 |
| **e** | 0.600 | 0.700 | 0.024 | 0.028 |
| **F** | 0.275 | 0.475 | 0.011 | 0.019 |
| **F1** | 0.000 | 0.100 | 0.000 | 0.004 |
| **L** | 0.520 | 0.720 | 0.020 | 0.028 |
| **L1** | 0.300 | 0.500 | 0.012 | 0.020 |
| **H** | 0.330 | 0.530 | 0.013 | 0.021 |
| **H1** | 0.200 | 0.400 | 0.008 | 0.016 |

## *SUGGESTED SOLDER PAD LAYOUT*

Unit:mm