

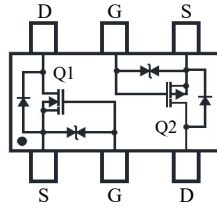
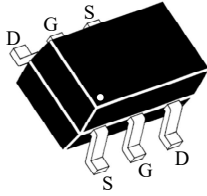


SMX8472KDW H

Complementary Pair Enhancement Mode Field Effect Transistors

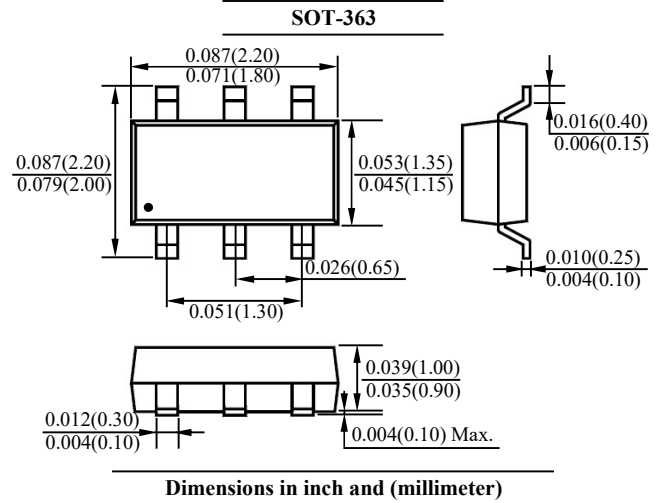
FEATURES

- ESD protected gate
- Suffix "H" indicates Halogen-free parts, ex.SMX8472KDW H



Top View

D	Drain
G	Gate
S	Source



Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Q1 Value	Q2 Value	Unit
Drain-Source Voltage	V_{DS}	60	-50	V
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Continuous Drain Current	I_D	0.30	-0.16	A
Peak Drain Current (Note 1)	I_{DM}	1.20	-0.64	A
Power Dissipation (Note 2)	P_D	250		mW
Thermal Resistance from Junction to Ambient (Note 2)	$R_{\theta JA}$	500		$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150		$^\circ\text{C}$

Note :

1. Pulse width $\leq 10\mu\text{s}$
2. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



SMX8472KDW H

Complementary Pair Enhancement Mode Field Effect Transistors

Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

N-Channel Q1

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static						
Drain Source Breakdown Voltage	$I_D = 10\mu\text{A}$	$V_{(BR)DSS}$	60	-	-	V
Gate Threshold Voltage	$V_{DS} = 10\text{V}, I_D = 250\mu\text{A}$	$V_{GS(th)}$	1.10	-	1.75	V
Zero Gate Voltage Drain Current	$V_{DS} = 60\text{V}$	I_{DSS}	-	-	1	μA
Gate-Body Leakage Current	$V_{GS} = \pm 20\text{V}$	I_{GSS}	-	-	± 10	μA
Drain-Source On-State Resistance	$V_{GS} = 10\text{V}, I_D = 0.5\text{A}$	$R_{DS(on)}$	-	-	3	Ω
	$V_{GS} = 5\text{V}, I_D = 0.05\text{A}$		-	-	4	
Dynamic						
Forward Transfer Admittance	$V_{DS} = 10\text{V}, I_D = 0.2\text{A}$	g_{FS}	80	-	-	mS
Gate Resistance	$V_{GS} = 0\text{V}, V_{DS} = 0\text{V}, f = 1\text{MHz}$	R_g	-	200	-	Ω
Total Gate Charge	$V_{DS} = 10\text{V}, V_{GS} = 4.5\text{V}, I_D = 0.5\text{A}$	Q_g	-	0.44	-	nC
Gate-Source Charge		Q_{gs}	-	0.20	-	
Gate-Drain Charge		Q_{gd}	-	0.10	-	
Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{iss}	-	22.5	50.0	pF
Output Capacitance		C_{oss}	-	12.0	25.0	
Reverse Transfer Capacitance		C_{rss}	-	0.5	10.0	
Turn-On Delay Time	$V_{DS} = 30\text{V}, V_{GS} = 10\text{V}, I_D = 0.5\text{A}, R_g = 25\Omega$	$t_{d(on)}$	-	2.7	-	ns
Turn-On Rise Time		t_r	-	2.5	-	
Turn-Off Delay Time		$t_{d(off)}$	-	13.0	-	
Turn-Off Fall Time		t_f	-	8.0	-	
Drain-Source Body Diode						
Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 0.5\text{A}$	V_{SD}	-	0.85	-	V
Diode Continuous Forward Current	-	I_S	-	-	0.3	A
Reverse Recovery Time	$I_S = 0.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	-	30	-	ns
Reverse Recovery Charge		Q_{rr}	-	29	-	nC



SMX8472KDW H

Complementary Pair Enhancement Mode Field Effect Transistors

Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

P-Channel Q2

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static						
Drain Source Breakdown Voltage	$I_D = -10\mu\text{A}$	$V_{(BR)DSS}$	-50	-	-	V
Zero Gate Voltage Drain Current	$V_{DS} = -50\text{V}$	I_{DSS}	-	-	-1	μA
Gate Source Leakage Current	$V_{GS} = \pm 20\text{V}$	I_{GSS}	-	-	± 10	μA
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	$V_{GS(th)}$	-1.1	-	-2.1	V
Static Drain Source On-Resistance	$V_{GS} = -10\text{V}, I_D = -0.1\text{A}$	$R_{DS(on)}$	-	-	7.5	Ω
	$V_{GS} = -5\text{V}, I_D = -0.1\text{A}$		-	-	8.5	
Dynamic						
Forward Transconductance	$V_{DS} = -10\text{V}, I_D = -0.1\text{A}$	g_{fs}	-	150	-	mS
Total Gate Charge	$V_{DS} = -25\text{V}, V_{GS} = -4.5\text{V}, I_D = -0.1\text{V}$	Q_g	-	1.1	-	nC
Gate-Source Charge		Q_{gs}	-	0.3	-	
Gate-Drain Charge		Q_{gd}	-	0.2	-	
Input Capacitance	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{iss}	-	38	-	pF
Output Capacitance		C_{oss}	-	9	-	
Reverse Transfer Capacitance		C_{rss}	-	6	-	
Turn-On Delay Time	$V_{DD} = -25\text{V}, V_{GS} = -10\text{V}, I_D = -0.1\text{A}, R_g = 6.8\Omega$	$t_{d(on)}$	-	14	-	ns
Turn-On Rise Time		t_r	-	4	-	
Turn-Off Delay Time		$t_{d(off)}$	-	15	-	
Turn-Off Fall Time		t_f	-	77	-	
Drain-Source Body Diode						
Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -0.115\text{A}$	V_{SD}	-0.48	-	-1.20	V
Continuous Source Current	-	I_S	-	-	-0.16	A
Reverse Recovery Time	$I_S = -0.1\text{A}, di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	-	60	-	ns
Reverse Recovery Charge		Q_{rr}	-	58	-	nC



SMX8472KDW

Complementary Pair Enhancement Mode Field Effect Transistors

RATINGS AND CHARACTERISTIC CURVES

N-Channel Q1

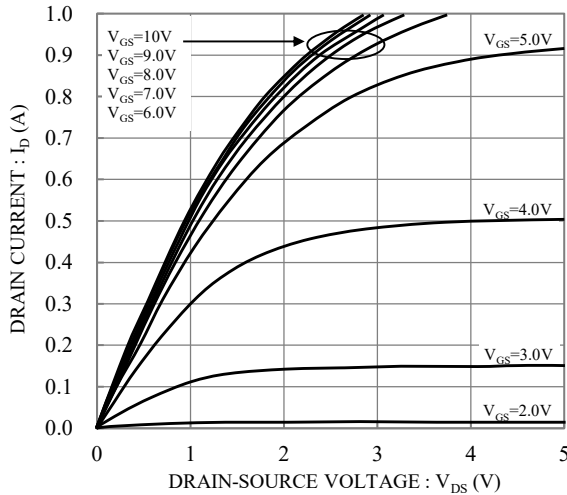


Fig.1 Typical Output Characteristics

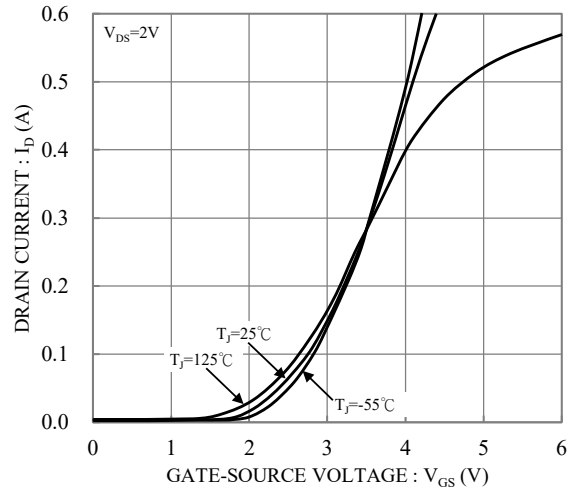


Fig.2 Typical Transfer Characteristics

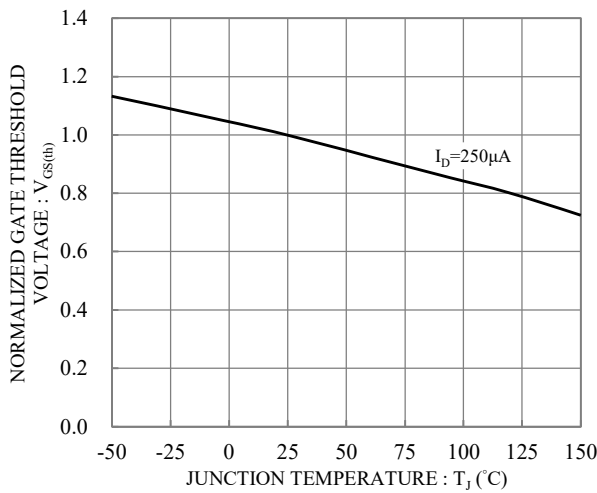


Fig.3 Gate Threshold Voltage vs. Junction Temperature

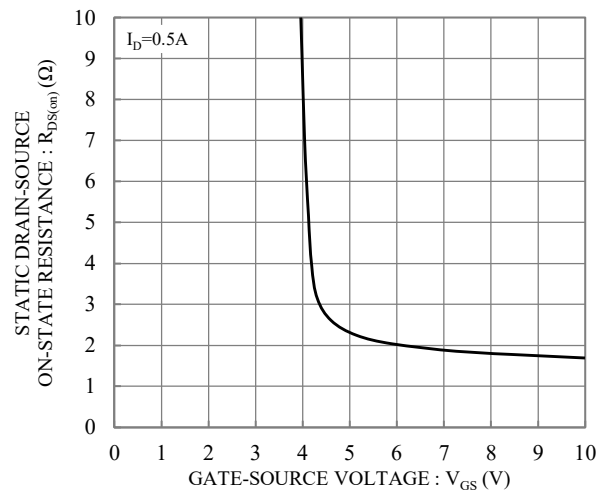


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

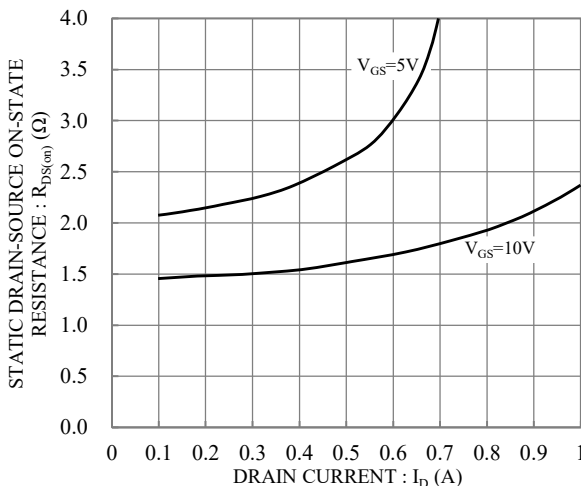


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

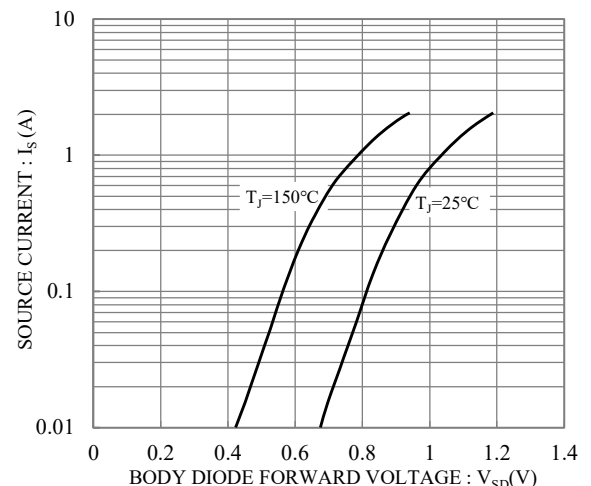


Fig.6 Body Diode Forward Voltage vs. Source Current



SMX8472KDW

Complementary Pair Enhancement Mode Field Effect Transistors

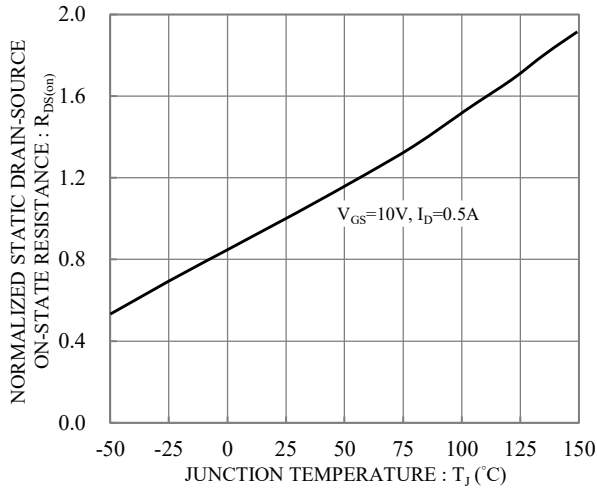


Fig.7 Drain-Source On-State Resistance vs. Junction Temperature

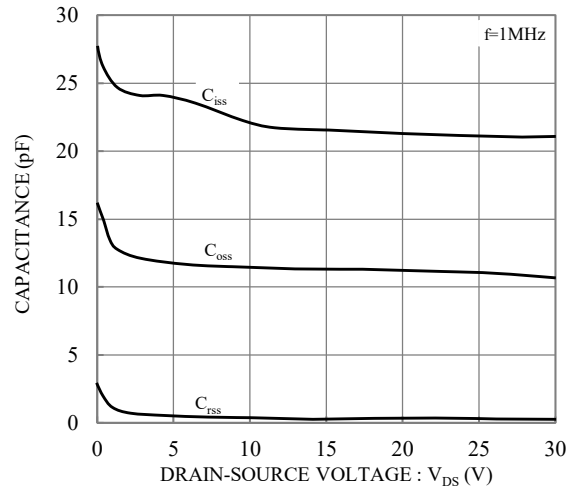


Fig.8 Capacitance vs. Drain-Source Voltage

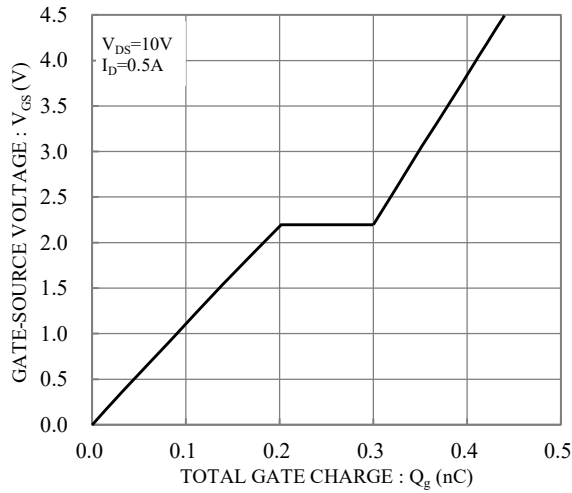


Fig.9 Gate Charge Characteristics



SMX8472KDW

Complementary Pair Enhancement Mode Field Effect Transistors

P-Channel Q2

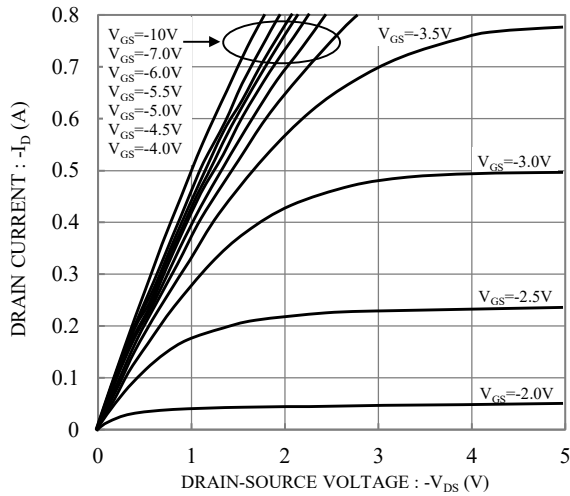


Fig.10 Typical Output Characteristics

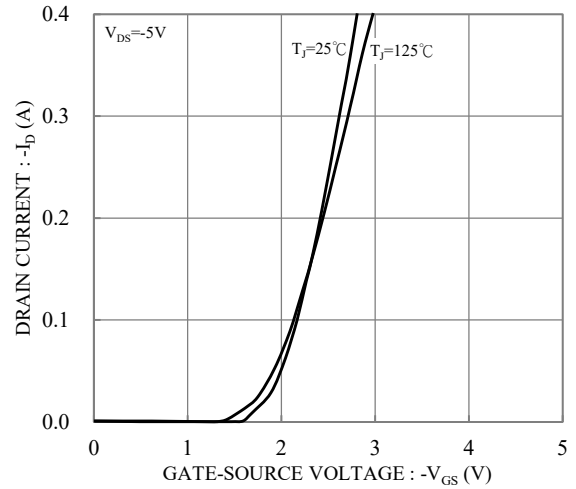


Fig.11 Typical Transfer Characteristics

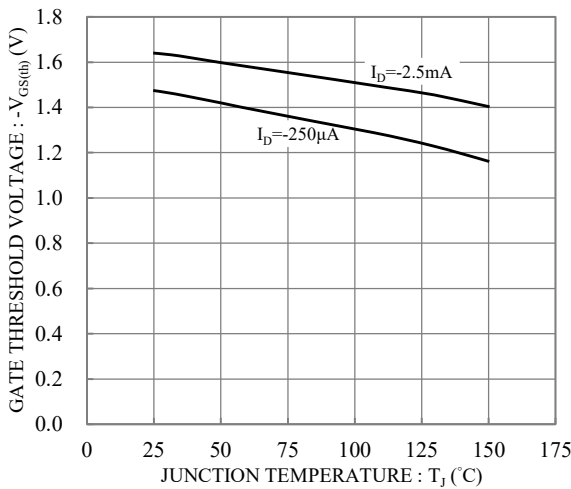


Fig.12 Gate Threshold Voltage vs. Junction Temperature

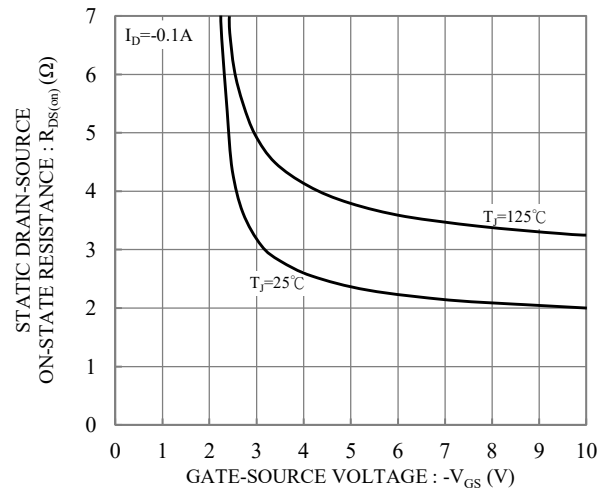


Fig.13 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

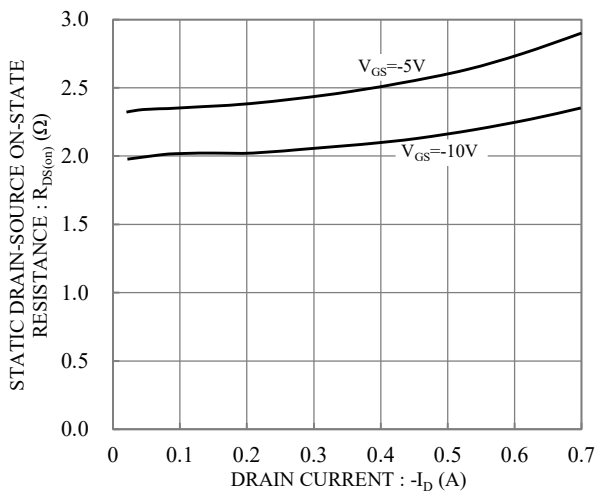


Fig.14 Static Drain-Source On-State Resistance vs. Drain Current

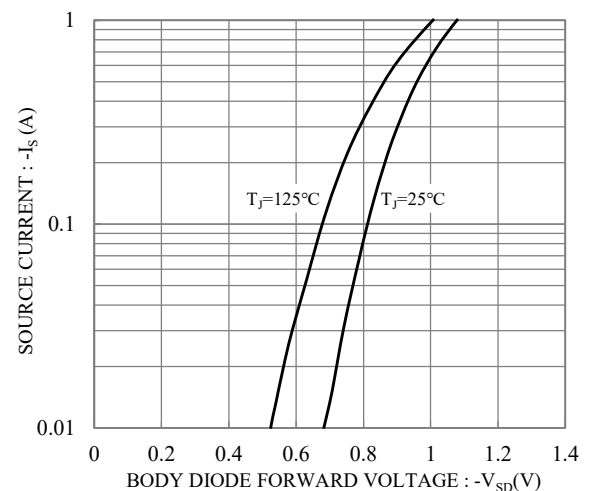


Fig.15 Body Diode Forward Voltage vs. Source Current



SMX8472KDW

Complementary Pair Enhancement Mode Field Effect Transistors

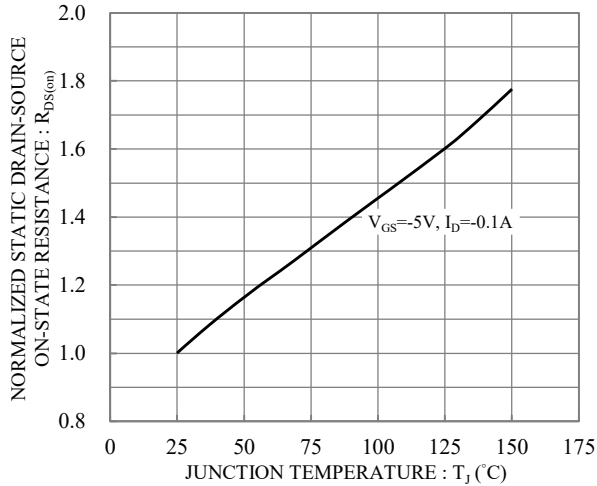


Fig.16 Drain-Source On-State Resistance vs. Junction Temperature

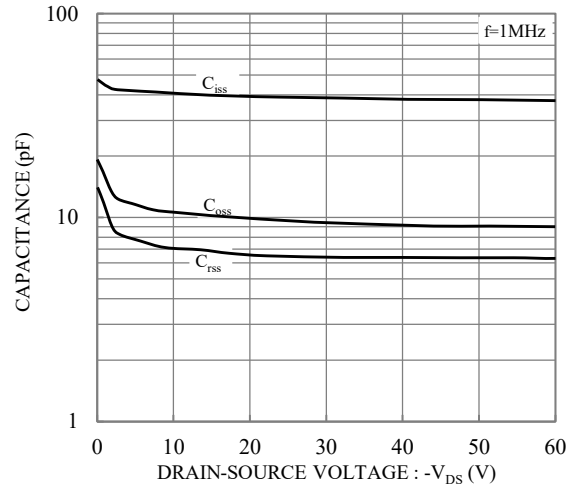


Fig.17 Capacitance vs. Drain-Source Voltage

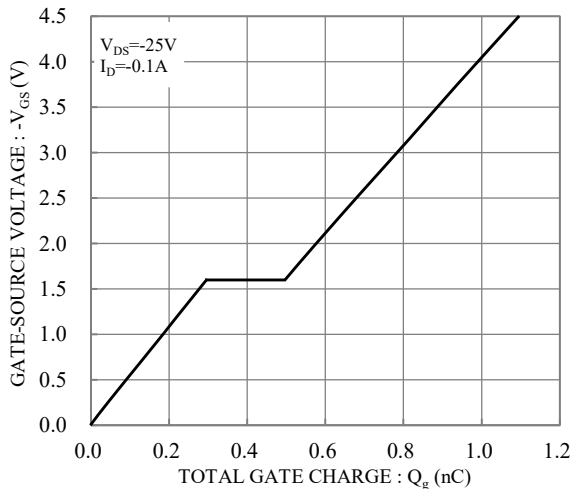


Fig.18 Gate Charge Characteristics

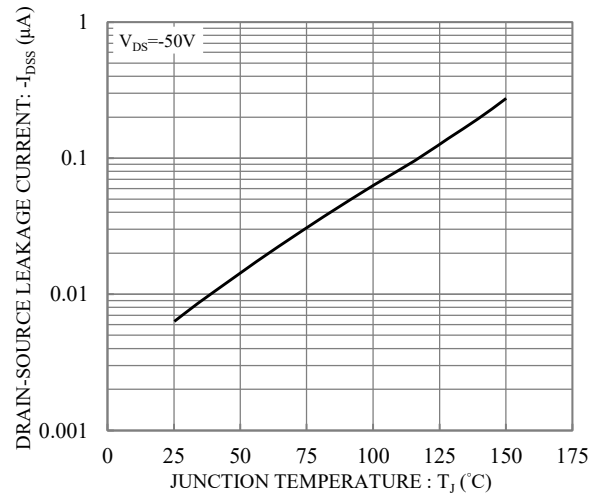


Fig.19 Drain-Source Leakage Current vs. Junction Temperature

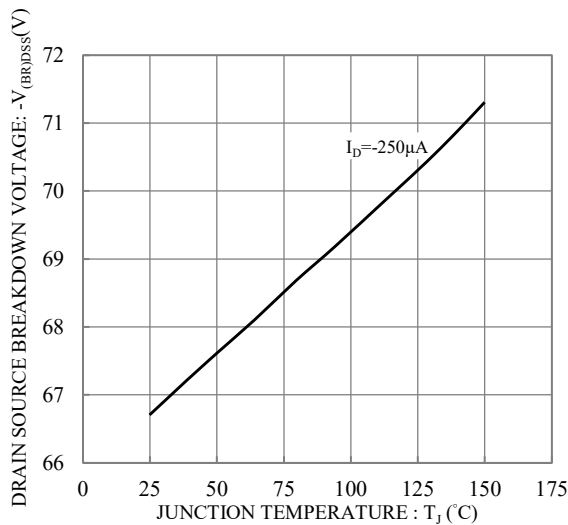


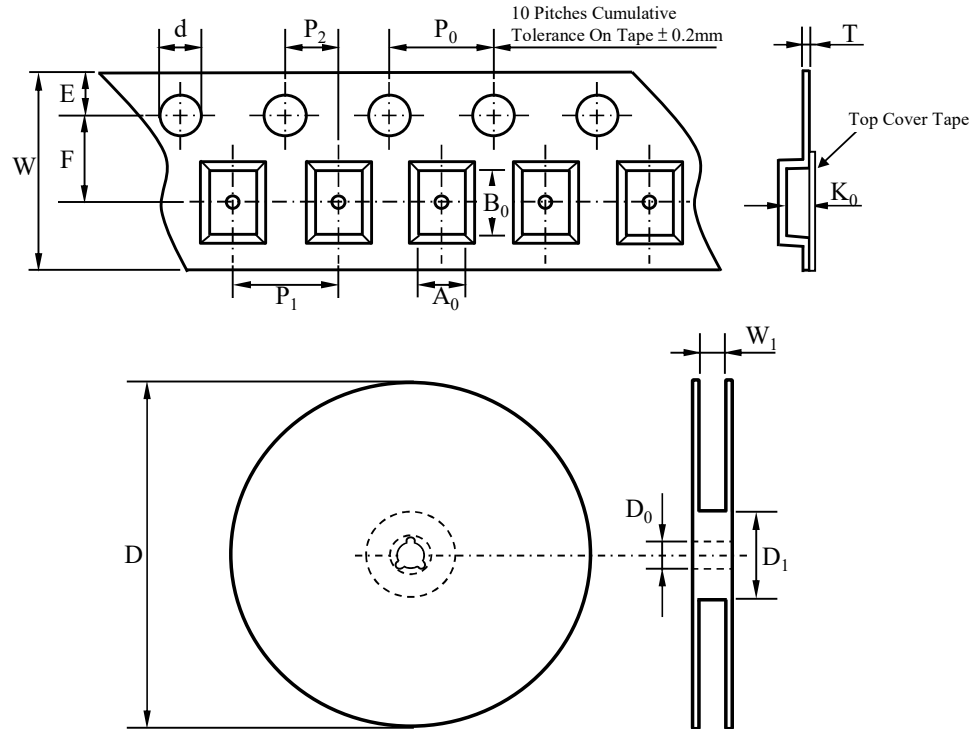
Fig.20 Drain Source Breakdown Voltage vs. Junction Temperature



SMX8472KDW H

Complementary Pair Enhancement Mode Field Effect Transistors

TAPE & REEL SPECIFICATION



Item	Symbol	SOT-363
Carrier width	A_0	*
Carrier length	B_0	
Carrier depth	K_0	
Sprocket hole	d	1.50 ± 0.10
Reel outside diameter	D	178.00 ± 2.00
Feed hole width	D_0	13.00 ± 0.50
Reel inner diameter	D_1	MIN. 54.00
Sprocket hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.10
Sprocket hole pitch	P_0	4.00 ± 0.10
Punch hole pitch	P_1	4.00 ± 0.10
Embossment center	P_2	2.00 ± 0.10
Overall tape thickness	T	MAX. 0.60
Tape width	W	MAX. 8.30
Reel width	W_1	8.40 ± 1.50

Note *: A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max.

ORDER INFORMATION

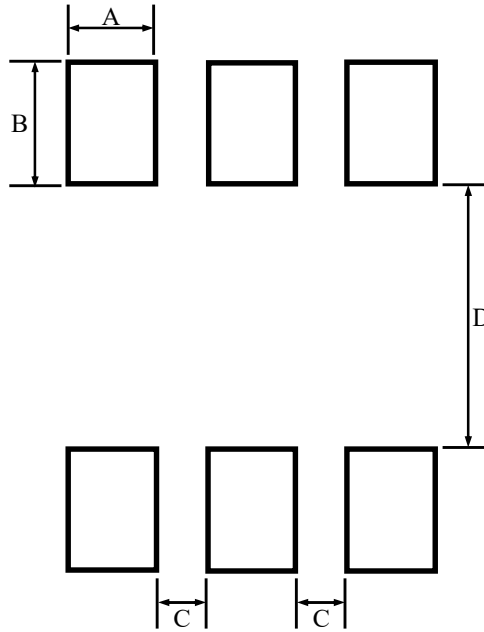
Part Number	Marking Code	Reel Size	Quantity
SMX8472KDW H	K8	7"	3,000



SMX8472KDW H

Complementary Pair Enhancement Mode Field Effect Transistors

SUGGESTED SOLDER PAD LAYOUT



Unit :mm

PACKAGE	A	B	C	D
SOT-363	0.42	0.60	0.23	1.30