



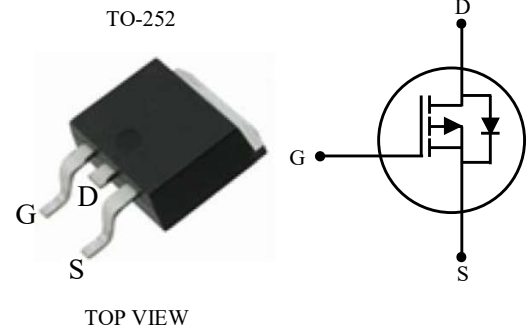
SMTR04P047SSK3H

P-Channel Enhancement Mode Field Effect Transistor

FEATURES

· Suffix "H" indicates Halogen-free parts, ex. SMTR04P047SSK3H

PIN CONFIGURATION



D	Drain
G	Gate
S	Source

Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current	I_D	$T_C = 25\text{ }^\circ\text{C}$	-64
		$T_C = 100\text{ }^\circ\text{C}$	-40
Pulsed Drain Current (Note 1)	I_{DM}	-350	A
Avalanche Current	I_{AS}	-66.5	A
Avalanche Energy (Note 2)	E_{AS}	221	mJ
Power Dissipation	P_D	48.3	W
Thermal Resistance from Junction to Ambient (Note 3)	$R_{\theta JA}$	38	$^\circ\text{C/W}$
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.5	$^\circ\text{C/W}$
Operating and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Note :

1. Pulse Test: Pulse Width $\leq 100\mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150\text{ }^\circ\text{C}$.
2. Limited by $T_{J(MAX)}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.1\text{mH}$, $R_g = 25\Omega$, $I_{AS} = -66.5\text{A}$, $V_{GS} = -10\text{V}$.
2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate in still air.



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Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static						
Drain Source Breakdown Voltage	$I_D = -250\mu\text{A}$	$V_{(BR)DSS}$	-40	-	-	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	$V_{GS(th)}$	-2.0	-	-4.0	V
Zero Gate Voltage Drain Current	$V_{DS} = -32\text{V}$	I_{DSS}	-	-	-1	μA
Gate-Body Leakage Current	$V_{GS} = \pm 16\text{V}$	I_{GSS}	-	-	± 0.1	μA
Drain-Source On-State Resistance	$V_{GS} = -10\text{V}, I_D = -30\text{A}$	$R_{DS(on)}$	-	6.4	7.6	$\text{m}\Omega$
Forward Transconductance	$V_{DS} = -5\text{V}, I_D = -10\text{A}$	g_{fs}	-	29	-	S
Dynamic						
Gate Resistance	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	R_g	-	2	-	Ω
Total Gate Charge	$V_{DS} = -20\text{V}, V_{GS} = -10\text{V}, I_D = -20\text{A}$	Q_g	-	105	-	nC
Gate-Source Charge		Q_{gs}	-	38	-	
Gate-Drain Charge		Q_{gd}	-	18	-	
Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{iss}	-	7475	-	pF
Output Capacitance		C_{oss}	-	555	-	
Reverse Transfer Capacitance		C_{rss}	-	329	-	
Turn-On Delay Time	$V_{GS} = -10\text{V}, V_{DD} = -20\text{V}, I_D = -20\text{A}, R_g = 3.3\Omega$	$t_{d(on)}$	-	44	-	ns
Turn-On Rise Time		t_r	-	52	-	
Turn-Off Delay Time		$t_{d(off)}$	-	30	-	
Turn-Off Fall Time		t_f	-	10	-	
Drain-Source Body Diode						
Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -1\text{A}$	V_{SD}	-	-	-1.2	V
Diode Continuous Source Current	-	I_S	-	-	-64	A
Diode Pulse Current		I_{SM}	-	-	-350	A
Reverse Recovery Time	$I_S = -20\text{A}, di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	-	26	-	ns
Reverse Recovery Charge		Q_{rr}	-	27	-	nC



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RATINGS AND CHARACTERISTIC CURVES

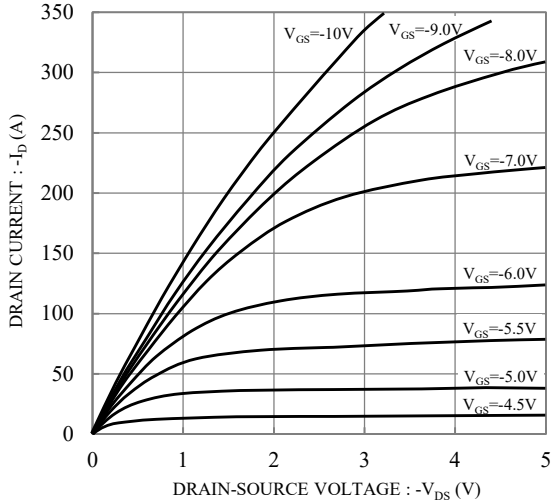


Fig.1 Typical Output Characteristics

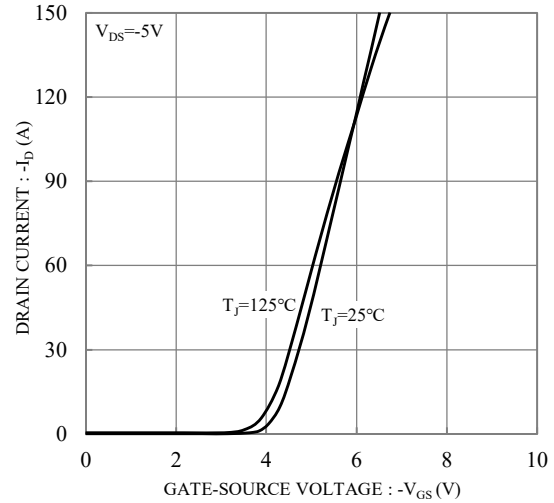


Fig.2 Typical Transfer Characteristics

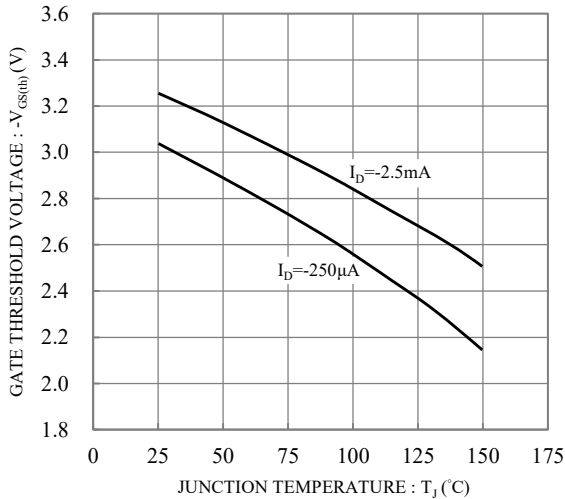


Fig.3 Gate Threshold Voltage vs. Junction Temperature

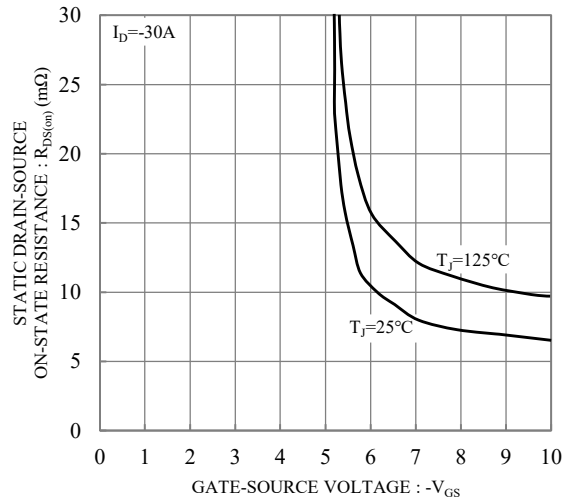


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

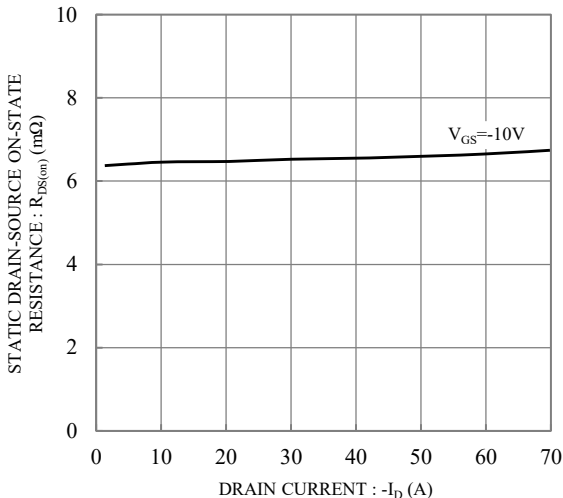


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

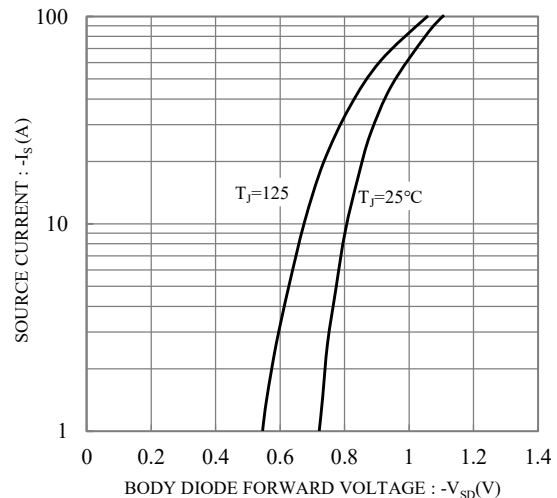


Fig.6 Body Diode Forward Voltage vs. Source Current



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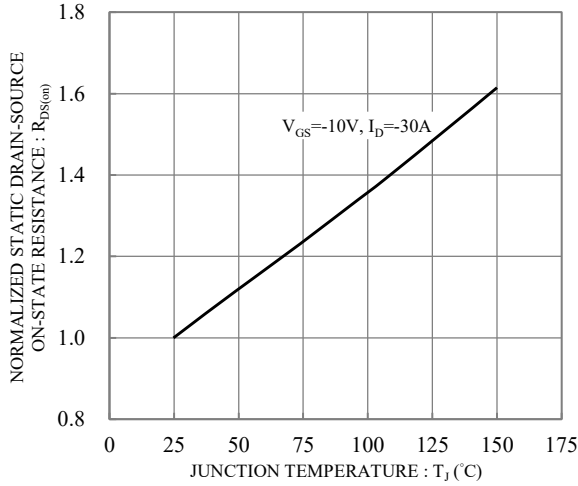


Fig.7 Drain-Source On-State Resistance vs. Junction Temperature

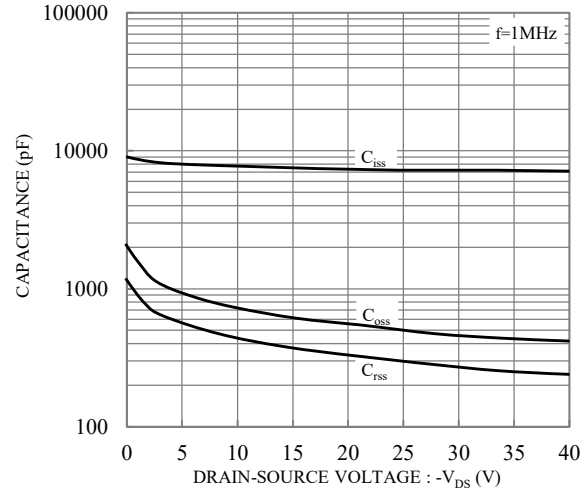


Fig.8 Capacitance vs. Drain-Source Voltage

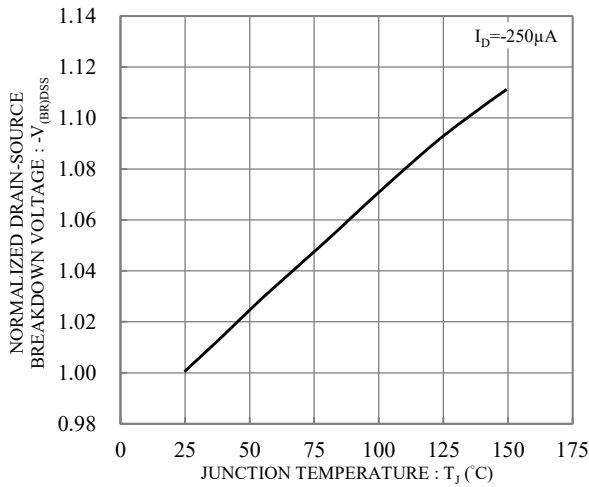


Fig.9 Breakdown Voltage vs. Junction Temperature

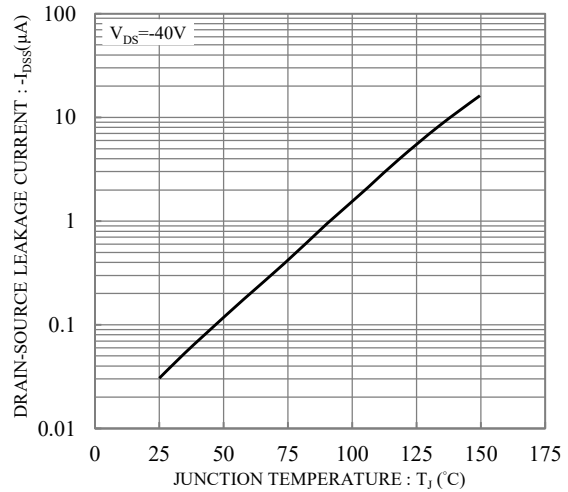


Fig.10 Drain-Source Leakage Current vs. Junction Temperature

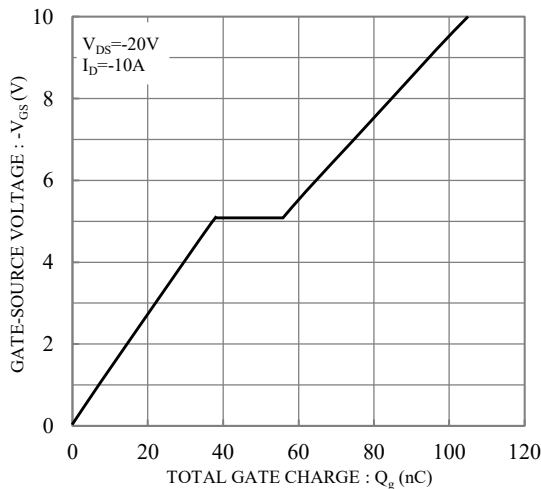


Fig.11 Gate Charge Characteristics

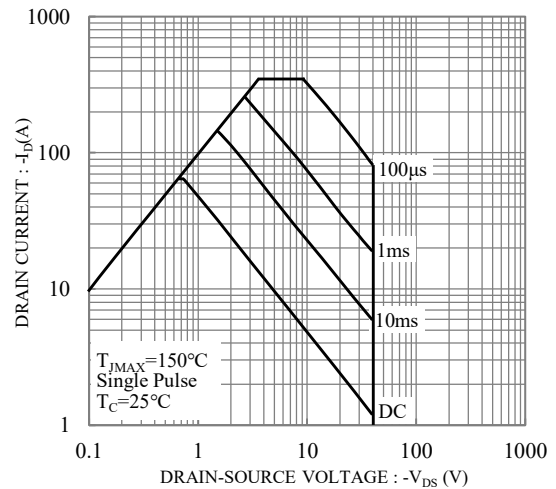


Fig.12 Drain-Source Leakage Current vs. Junction Temperature



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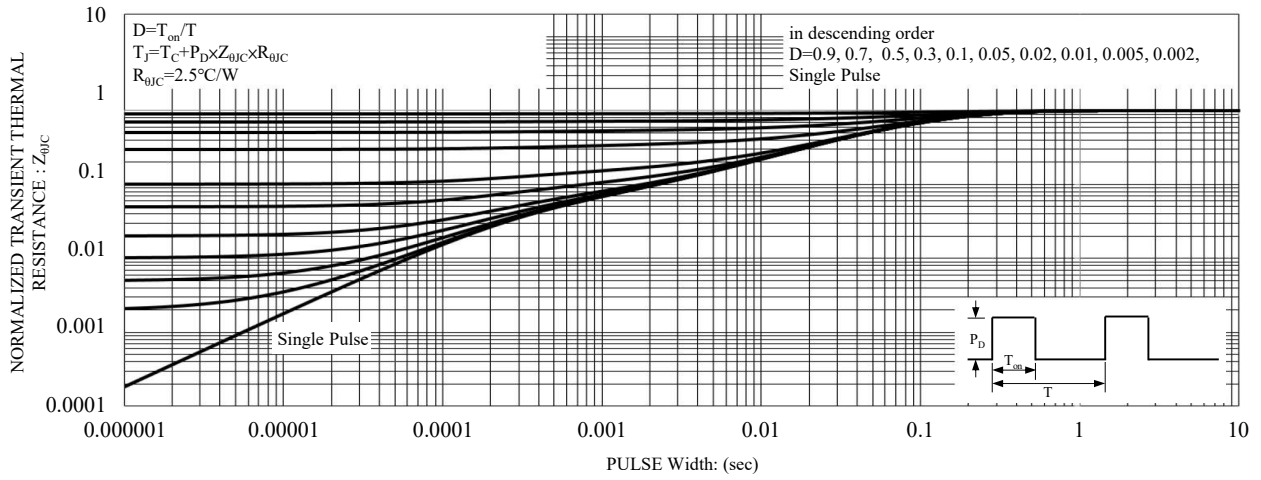


Fig.13 Maximum Transient Thermal Impedance

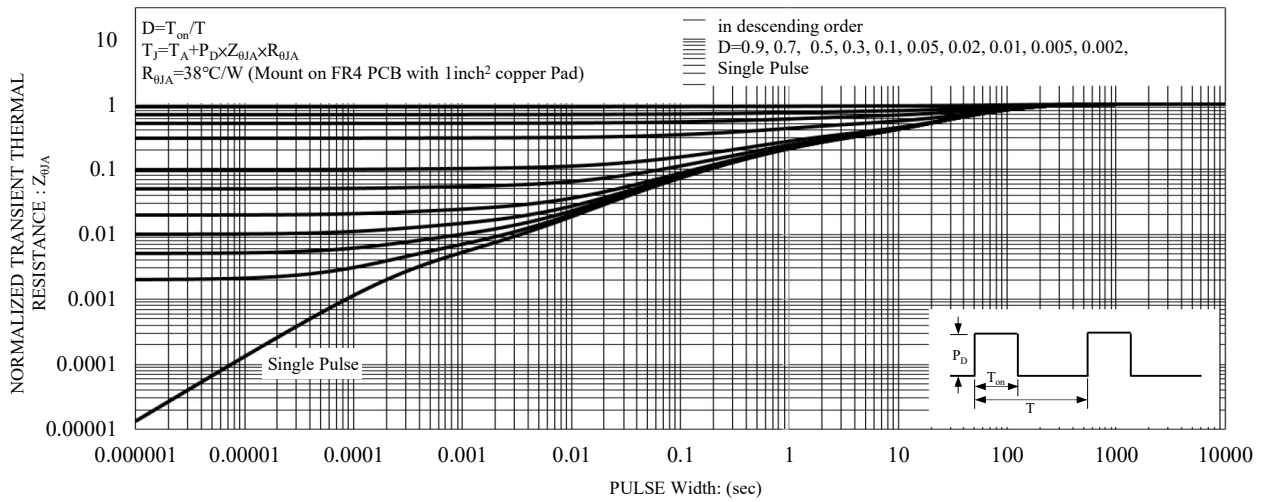


Fig.14 Maximum Transient Thermal Impedance

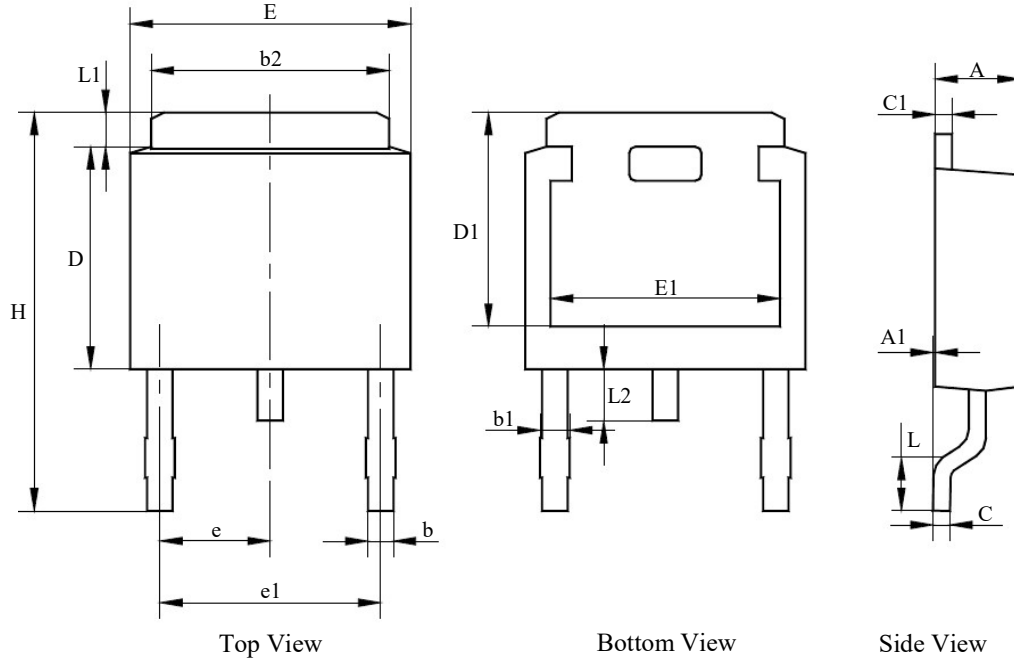


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PACKAGE DIMENSION

TO-252



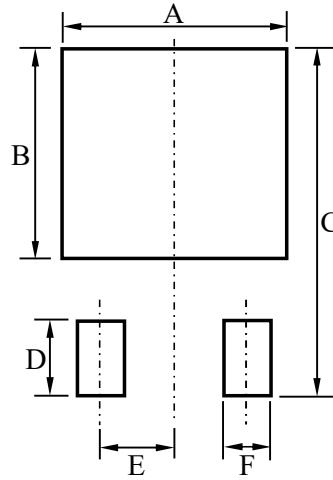
Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.10	2.50	0.083	0.098
A1	0.00	0.15	0.000	0.006
b	0.50	1.00	0.020	0.039
b1	0.65	1.15	0.026	0.045
b2	4.90	5.50	0.193	0.217
C	0.40	0.65	0.016	0.026
C1	0.40	0.65	0.016	0.026
D	5.60	6.20	0.220	0.244
D1	5.00	5.40	0.197	0.213
E	6.10	6.70	0.240	0.264
E1	4.60	5.00	0.181	0.197
e	Typ. 2.30		Typ. 0.091	
e1	Typ. 4.60		Typ. 0.181	
H	9.00	10.70	0.354	0.421
L	1.40	1.78	0.055	0.070
L1	0.85	1.20	0.033	0.047
L2	0.51	1.10	0.020	0.043



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SUGGESTED SOLDER PAD LAYOUT



Unit :mm

PACKAGE	A	B	C	D	E	F
TO-252	7.00	7.00	11.60	2.50	2.30	1.50