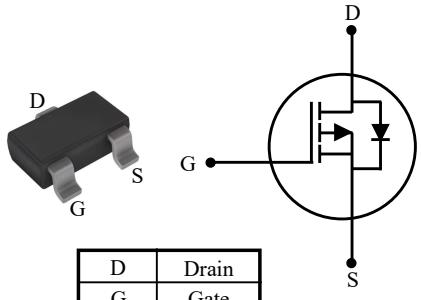
SMP5618TDSH

P-Channel Enhancement Mode Field Effect Transistor

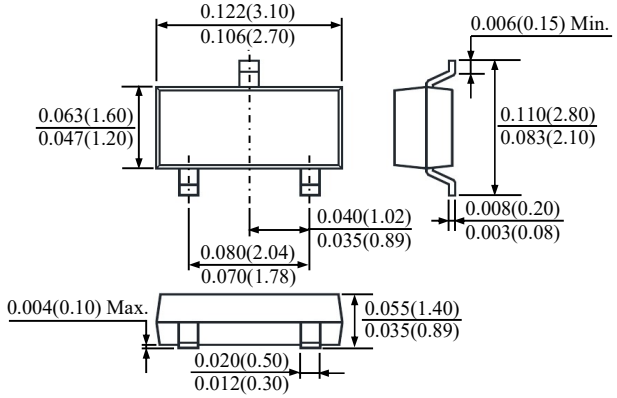
FEATURES

· Suffix "H" indicates Halogen-free parts, ex. SMP5618TDSH



D	Drain
G	Gate
S	Source

SOT-23



Dimensions in inch and (millimeter)

Maximum Ratings(T_A=25 ℃ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	±20	V
Drain Current	I_D	-1.25	A
Pulsed Drain Current (Note 1)	I_{DM}	-10	A
Power Dissipation (Note 2)	P_D	0.5	W
Thermal Resistance Juntion to Ambient (Note 2)	$R_{\theta JA}$	250	℃/W
Operating and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	℃

Note :

1. Pulse test : Pulse width≤100μs, duty cycle≤2%, repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=150℃
2. Device mounted on FR-4 substrate PC board, with minimum recommended pad layout.

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Electrical Characteristics(T_A=25 ℃ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static						
Drain Source Breakdown Voltage	I_D=-250μA	$V_{(BR)DSS}$	-60	-	-	V
Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250μA	$V_{GS(th)}$	-1.0	-	-3.0	V
Zero Gate Voltage Drain Current	V_{DS}=-48V	I_{DSS}	-	-	-1	μA
Gate-Body Leakage Current	V_{GS}=±20V	I_{GSS}	-	-	±100	nA
Drain-Source On-State Resistance	V_{GS}=-10V, I_D=-1.25A	$R_{DS(on)}$	-	-	170	mΩ
	V_{GS}=-4.5V, I_D=-1A		-	-	230	
Forward Transconductance	V_{DS}=-5V, I_D=-1.25A	g_{FS}	-	6	-	S
Dynamic						
Gate Resistance	V_{DS}=0V, V_{GS}=0V, f=1MHz	R_g	-	9.2	-	Ω
Total Gate Charge	V_{DS}=-30V, V_{GS}=-4.5V, I_D=-1.25A	Q_g	-	3.2	-	nC
	V_{DS}=-30V, V_{GS}=-10V, I_D=-1.25A		-	7.0	-	
Gate-Source Charge		Q_{gs}	-	1.6	-	
Gate-Drain Charge		Q_{gd}	-	1.3	-	
Input Capacitance	V_{DS}=-30V, V_{GS}=0V, f=1MHz	C_{iss}	-	361	-	pF
Output Capacitance		C_{oss}	-	25	-	
Reverse Transfer Capacitance		C_{rss}	-	20	-	
Turn-On Delay Time	V_{DD}=-30V, V_{GS}=-10V, I_D=-1.25A, R_g=3.3Ω	$t_{d(on)}$	-	5.7	-	ns
Turn-On Rise Time		t_r	-	3.4	-	
Turn-Off Delay Time		$t_{d(off)}$	-	7.5	-	
Turn-Off Fall Time		t_f	-	1.8	-	
Drain-Source Body Diode						
Drain-Source Diode Forward Voltage	I_S=-0.42A, V_{GS}=0V	V_{SD}	-	-	-1.2	V
Diode Continuous Forward Current	-	I_S	-	-	-1.25	A
Reverse Recovery Time	I_S=-1.25A, dI/dt=100A/μs	t_{rr}	-	8	-	ns
Reverse Recovery Charge		Q_{rr}	-	3.6	-	nC

RATINGS AND CHARACTERISTIC CURVES

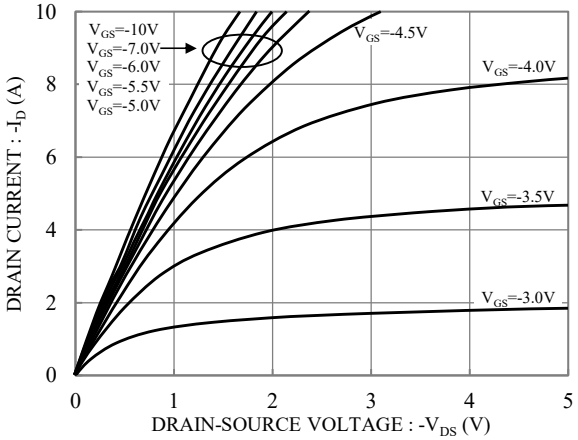


Fig.1 Typical Output Characteristics

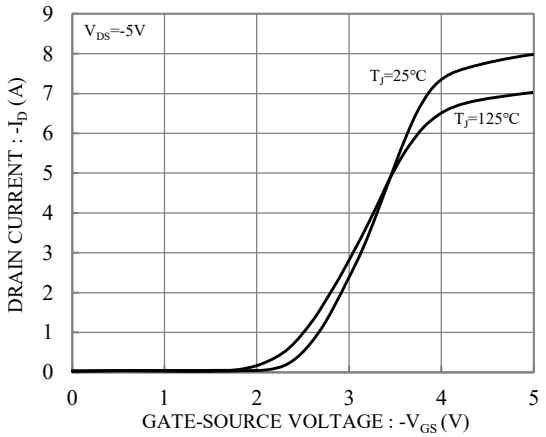


Fig.2 Typical Transfer Characteristics

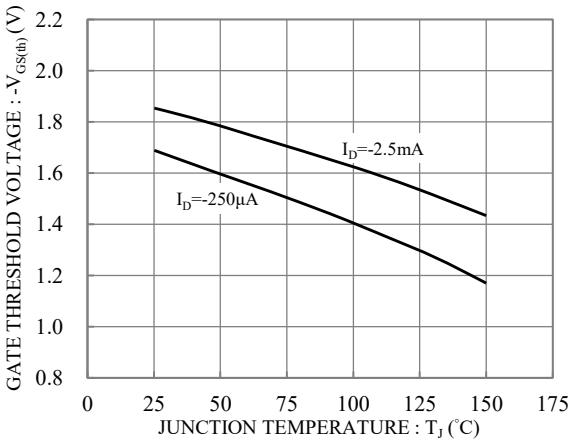


Fig.3 Gate Threshold Voltage vs. Junction Temperature

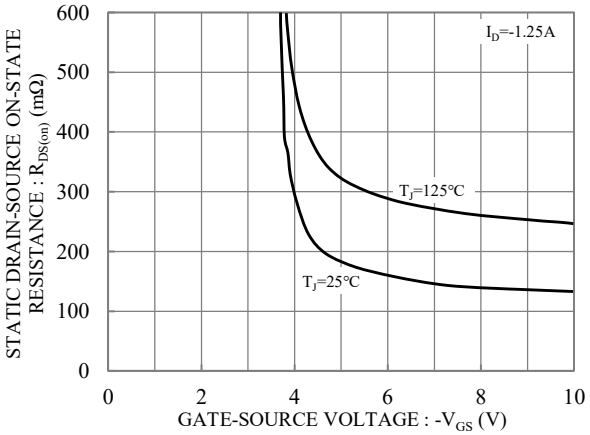


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

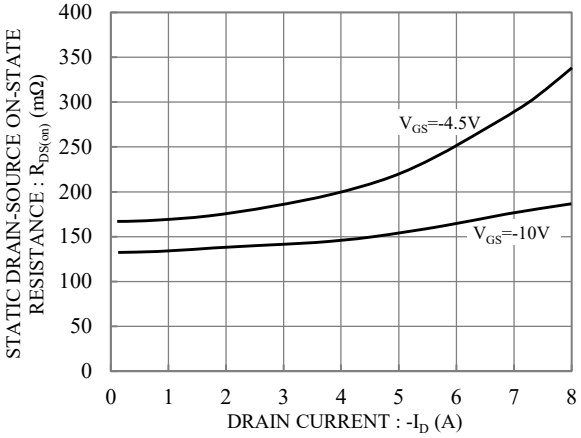


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

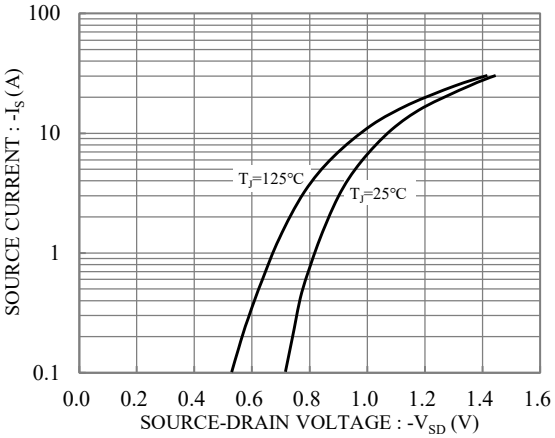


Fig.6 Diode Forward Voltage vs. Source Current

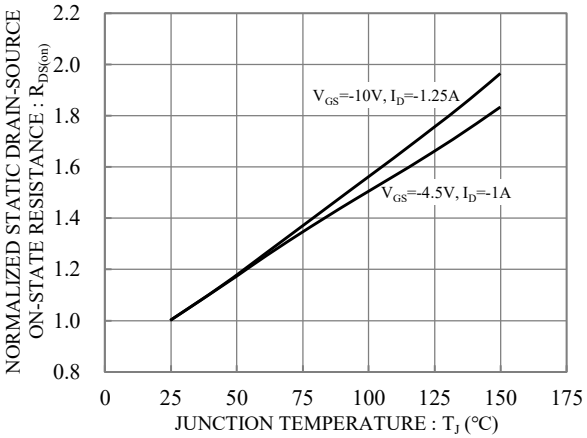


Fig.7 Normalized Static Drain-Source On-state Resistance vs. Junction Temperature

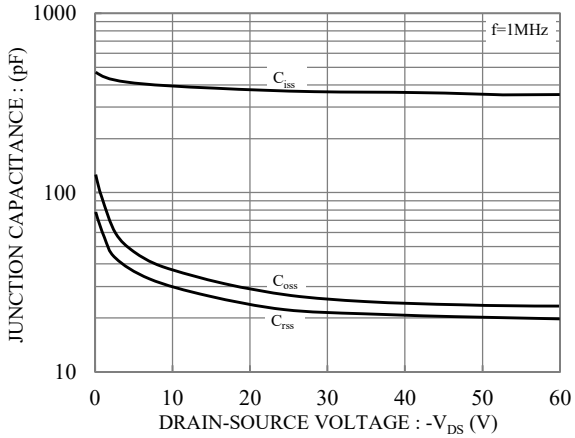


Fig.8 Capacitance vs. Drain-Source Voltage

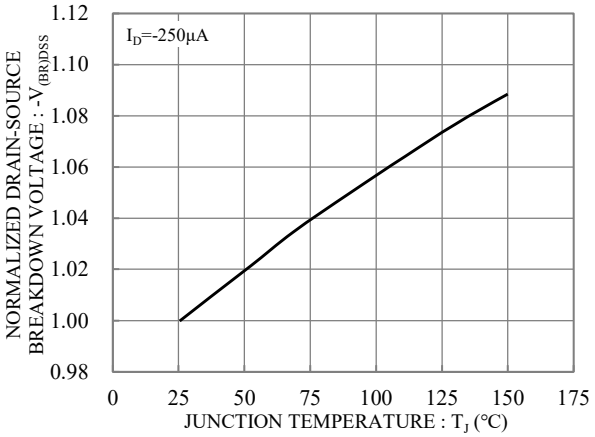


Fig.9 Breakdown Voltage vs. Junction Temperature

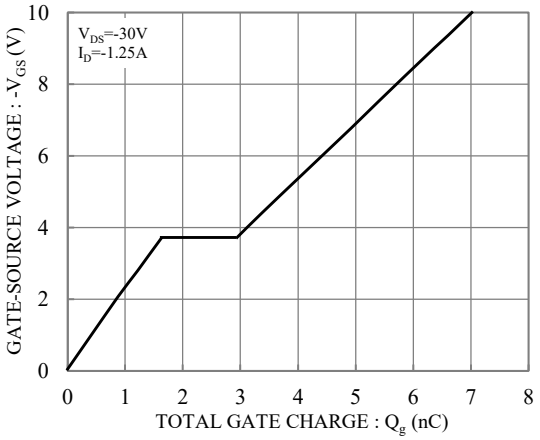


Fig.10 Gate Charge Characteristics

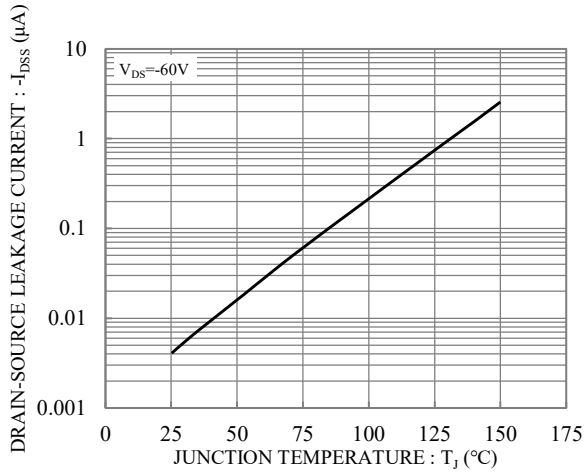
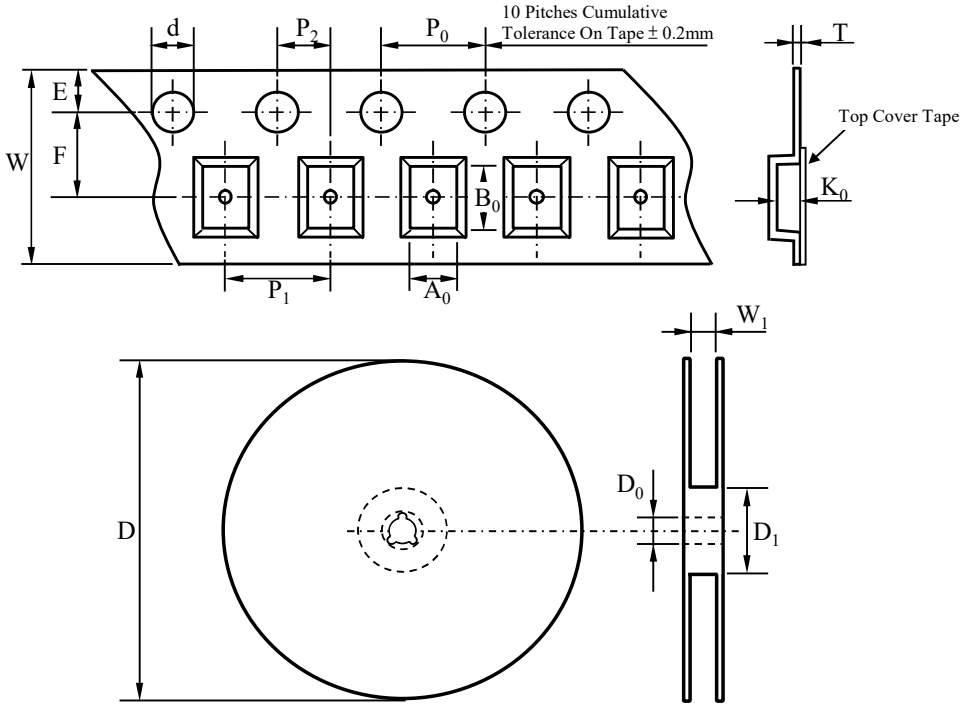


Fig.11 Drain-Source Leakage Current vs. Junction Temperature

TAPE & REEL SPECIFICATION



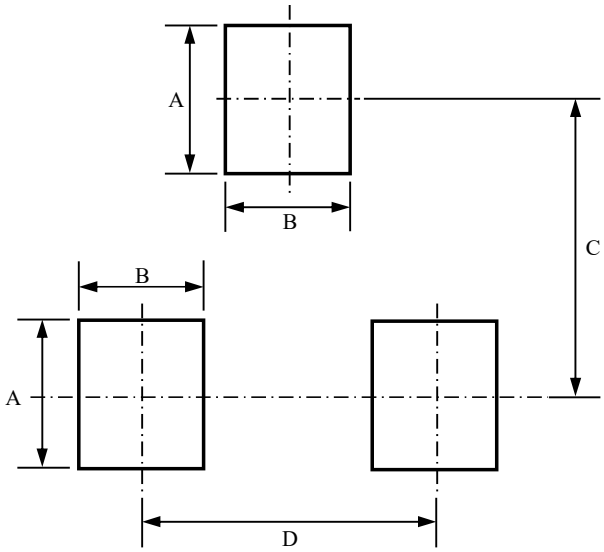
Item	Symbol	SOT-23
Carrier width	A_0	*
Carrier length	B_0	
Carrier depth	K_0	
Sprocket hole	d	1.50 ± 0.10
Reel outside diameter	D	178.00 ± 2.00
Feed hole width	D_0	13.00 ± 0.50
Reel inner diameter	D_1	MIN. 50.00
Sprocke hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.10
Sprocke hole pitch	P_0	4.00 ± 0.10
Punch hole pitch	P_1	4.00 ± 0.10
Embossment center	P_2	2.00 ± 0.10
Overall tape thickness	T	0.20 ± 0.05
Tape width	W	8.00 ± 0.20
Reel width	W1	MAX. 14.50

Note *: A_0, B_0, and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max.

ORDER INFORMATION

Part Number	Marking Code	Reel Size	Quantity
SMP5618TDSH	WQ	7"	3,000

SUGGESTED SOLDER PAD LAYOUT



Unit :mm

PACKAGE	A	B	C	D
SOT-23	1.00	0.80	2.00	1.90