



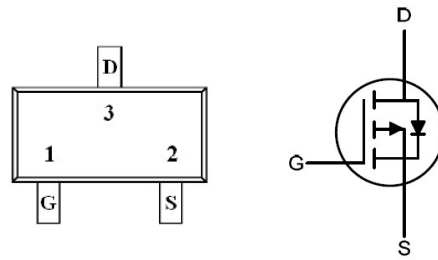
# SM6911IDS

## P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- $R_{DS(ON)} \leq 180m\Omega @ V_{GS} = -10V$
- $BV \leq -60V, I_D \leq -1.9A$
- Super Low Gate Charge
- Suffix "H" indicates Halogen-free parts, ex. SM6911IDSH

### PIN CONFIGURATION



Pin	Description
1	Gate
2	Source
3	Drain

### Maximum Ratings ( $T_A = 25^\circ C$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	$V_{DS}$	-60	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current, $V_{GS} = -10V$ (Note 1)	$I_D$	$T_A = 25^\circ C$	-1.9	A
		$T_A = 70^\circ C$	-1.4	
Pulsed Drain Current, $V_{GS} = -10V$ (Note 2)	$I_{DM}$	-7.6	A	
Power Dissipation (Note 3)	$P_D$	$T_A = 25^\circ C$	1.00	W
		$T_C = 25^\circ C$	1.56	
Thermal Maximum Junction to Ambient (Note 1)	$R_{\theta JA}$	125	$^\circ C/W$	
Thermal Maximum Junction to Case	$R_{\theta JC}$	80	$^\circ C/W$	
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	- 55 to + 150	$^\circ C$	

Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.  $t \leq 10SEC$
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$
3. Power dissipation is limited by 150 $^\circ C$  junction temperature



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### Electrical Characteristics ( $T_A=25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	$V_{(BR)DSS}$	-60	-	-	V
Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	$V_{GS(th)}$	-1.0	-	-2.5	V
Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	$I_{GSS}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS}=-48V, V_{GS}=0V$	$I_{DSS}$	-	-	-1	$\mu A$
	$V_{DS}=-48V, V_{GS}=0V, T_J=55^\circ C$		-	-	-5	
Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-1.5A$	$R_{DS(on)}$	-	-	180	m $\Omega$
	$V_{GS}=-4.5V, I_D=-1.0A$		-	-	266	
Diode Forward Voltage (Note 2)	$V_{DS}=-5V, I_D=-1.5A$	$g_{FS}$	-	5.9	-	S
<b>Dynamic (Note 4)</b>						
Total Gate Charge	$V_{DS}=-0V, V_{GS}=-4.5V, I_D=-1.5A$	$Q_g$	-	4.60	-	nC
Gate-Source Charge		$Q_{gs}$	-	1.40	-	
Gate-Drain Charge		$Q_{gd}$	-	1.62	-	
Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	$C_{iss}$	-	531	-	pF
Output Capacitance		$C_{oss}$	-	59	-	
Reverse Transfer Capacitance		$C_{rss}$	-	38	-	
Turn on Delay Time		$t_{d(on)}$	-	17.4	-	
Turn on Rise Time	$V_{DS}=-15V, I_D=-1A$	$t_r$	-	5.4	-	
Turn off Delay Time	$V_{GS}=-10V, R_G=3.3\Omega$	$t_{d(off)}$	-	37.2	-	
Turn off Fall Time	$t_f$	-	2.4	-		
<b>Drain-Source Body Diode</b>						
Diode Forward Voltage	$V_{GS}=0V, I_S=-1A$	$V_{SD}$	-	-	-1.2	V

Note:

4. Guarantee by design, not test in mass production.



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### RATINGS AND CHARACTERISTIC CURVES

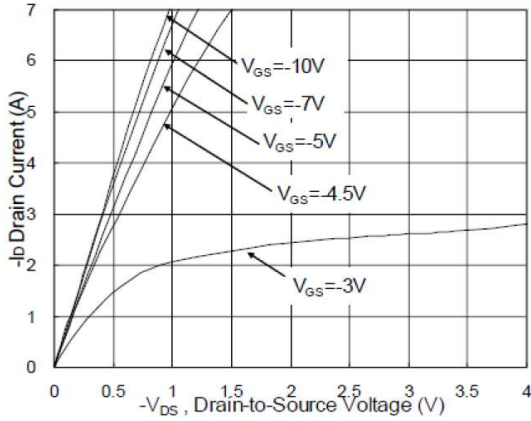


Fig.1 Typical Output Characteristics

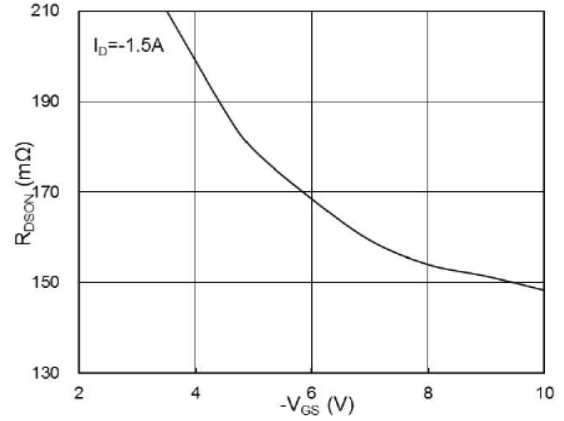


Fig.2 On Resistance vs. Gate Source

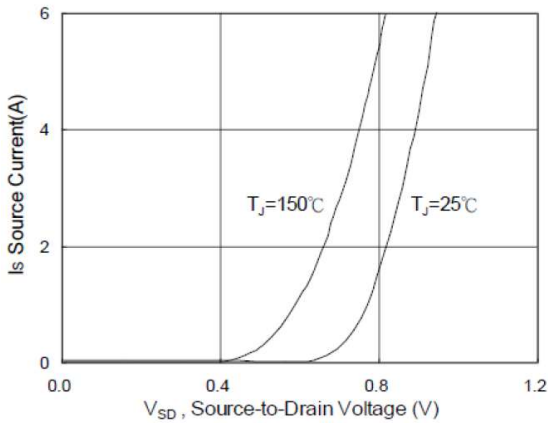


Fig.3 Forward Characteristics Of Reverse

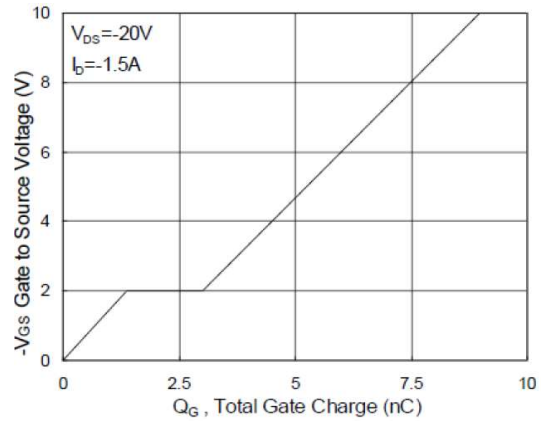


Fig.4 Gate Charge Characteristics

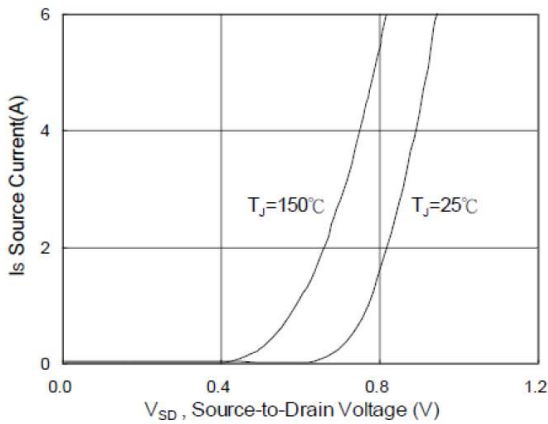


Fig.5 Normalized  $V_{GS(th)}$  vs.  $T_J$

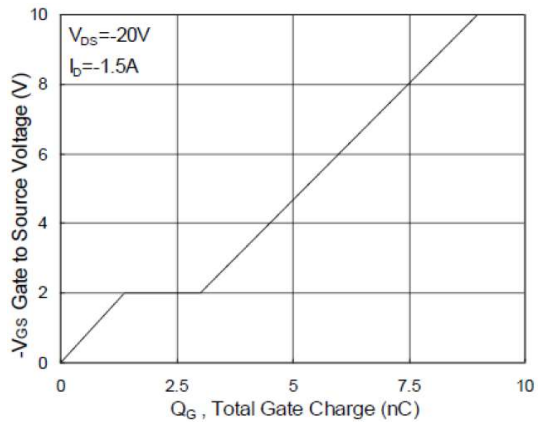


Fig.6 Normalized  $R_{DS(on)}$  vs.  $T_J$



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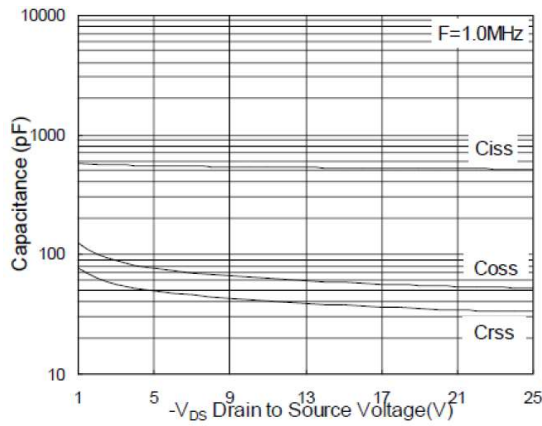


Fig.7 Capacitance

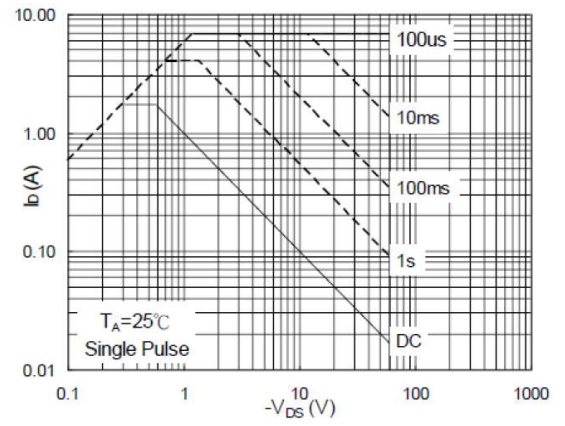


Fig.8 Safe Operating Area

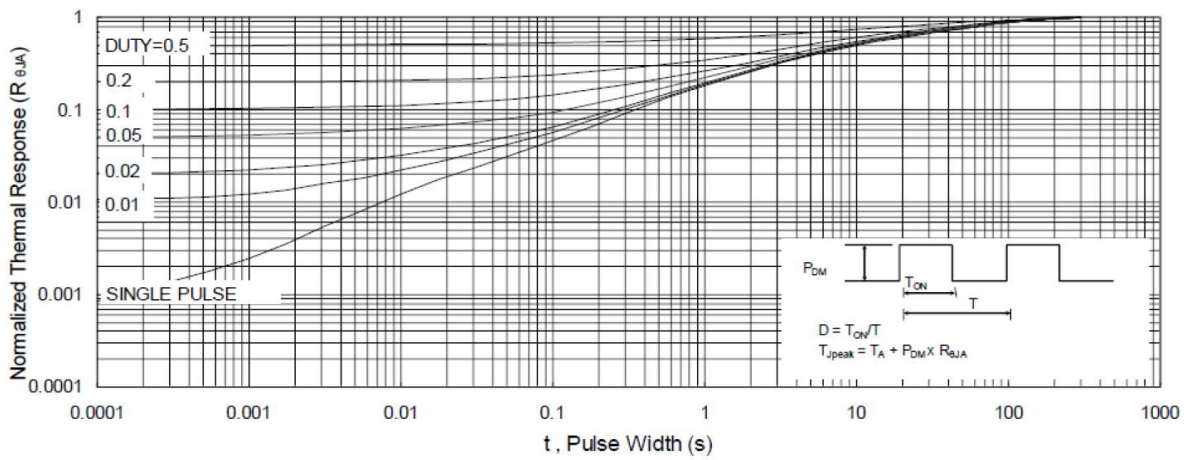


Fig.9 Normalized Maximum Transient Thermal Impedance

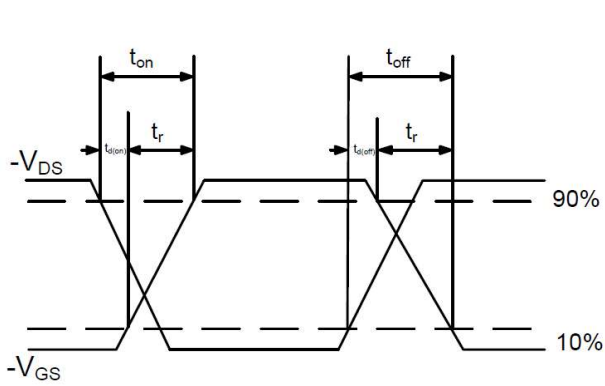


Fig.10 Switching Time Waveform

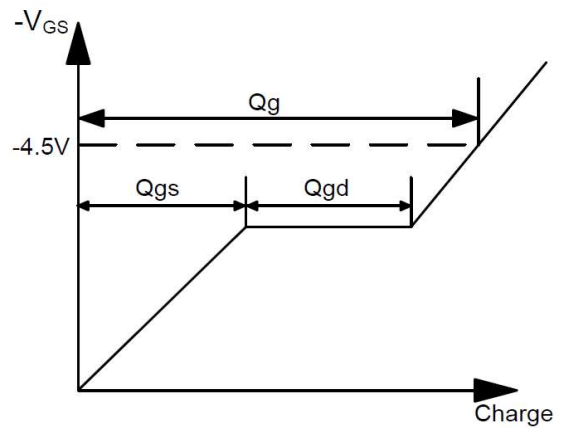


Fig.11 Gate Charge waveform

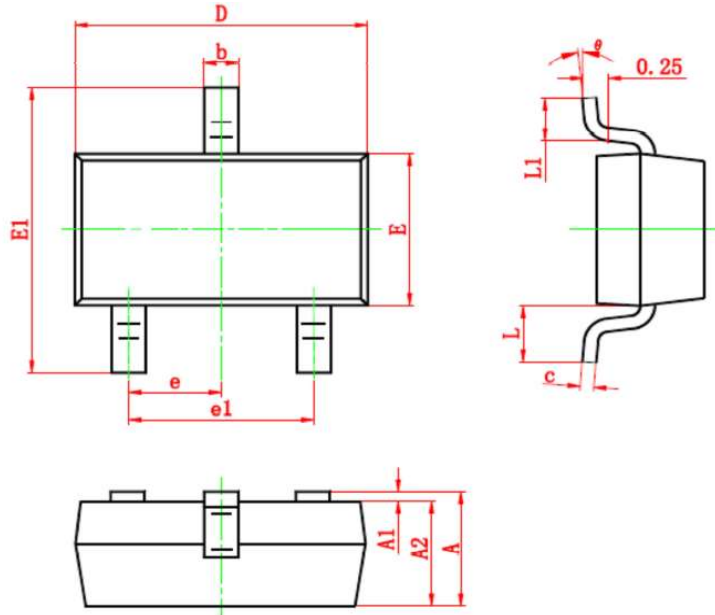


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## P-Channel Enhancement Mode Field Effect Transistor

### Package Dimension

### SOT-23



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.15	0.035	0.045
A1	0.00	0.10	0.000	0.004
A2	0.90	1.05	0.035	0.041
b	0.30	0.50	0.012	0.020
c	0.08	0.15	0.003	0.006
D	2.80	3.00	0.110	0.118
E	1.20	1.40	0.047	0.055
E1	2.25	2.55	0.089	0.100
e	TYP 0.95		TYP 0.037	
e1	1.80	2.00	0.071	0.079
L	REF 0.55		REF 0.022	
L1	0.30	0.50	0.012	0.020
θ	0°	8°	0°	8°