



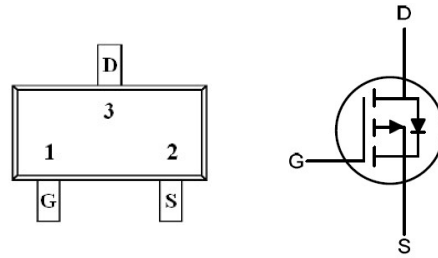
# SM3911IDS

## P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- $R_{DS(ON)}=60m\Omega@V_{GS}=-10V$
- $R_{DS(ON)}=100m\Omega@V_{GS}=-4.5V$
- Suffix "H" indicates Halogen-free parts, ex. SM3911IDSH

### PIN CONFIGURATION



Pin	Description
1	Gate
2	Source
3	Drain

### Maximum Ratings( $T_A=25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$T_A=25^\circ\text{C}$ $V_{DS}$	-30	V
Gate-Source Voltage	$T_A=25^\circ\text{C}$ $V_{GS}$	$\pm 20$	
Continuous Drain Current, $V_{GS}=-10V$ (Note 1)	$T_A=25^\circ\text{C}$ $I_D$	-3.0	A
	$T_A=100^\circ\text{C}$	-1.9	
Pulsed Drain Current, $V_{GS}=-10V$ (Note 2)	$T_A=25^\circ\text{C}$ $I_{DM}$	-12	A
Power Dissipation (Note 3)	$T_A=25^\circ\text{C}$ $P_D$	1.00	W
	$T_C=25^\circ\text{C}$	1.56	
Thermal Maximum Junction to Ambient (Note 1)	$R_{\theta JA}$	125	$^\circ\text{C/W}$
Thermal Maximum Junction to Case	$R_{\theta JC}$	80	$^\circ\text{C/W}$
Operating Junction and Storage Temperature Range	$T_j, T_{stg}$	- 55 to + 150	$^\circ\text{C}$

Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.  $t \leq 10\text{SEC}$
2. The data tested by pulsed , pulse width  $\leq 300\mu\text{s}$  , duty cycle  $\leq 2\%$
3. Power dissipation is limited by 150 $^\circ\text{C}$  junction temperature



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### Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	$V_{(BR)DSS}$	-30	-	-	V
Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	$V_{GS(th)}$	-1.2	-	-2.2	V
Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$	$I_{GSS}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$	$I_{DSS}$	-	-	-1	$\mu A$
	$V_{DS}=-24V, V_{GS}=0V, T_J=85^\circ C$		-	-	-30	
Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-3A$	$R_{DS(on)}$	-	45	60	m $\Omega$
	$V_{GS}=-4.5V, I_D=-2A$		-	70	100	
<b>Dynamic (Note 4)</b>						
Total Gate Charge	$V_{DS}=-15V, V_{GS}=-10V, I_D=-3A$	$Q_g$	-	13.2	-	nC
Gate-Source Charge		$Q_{gs}$	-	2.4	-	
Gate-Drain Charge		$Q_{gd}$	-	2.0	-	
Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1MHz$	$C_{iss}$	-	619	1005	pF
Output Capacitance		$C_{oss}$	-	125	188	
Reverse Transfer Capacitance		$C_{rss}$	-	65	32.6	
Turn on Delay Time		$t_{d(on)}$	-	2.6	-	
Turn on Rise Time	$V_{DD}=-15V, R_L=5\Omega, I_D=-3A$	$t_r$	-	7.8	-	nS
Turn off Delay Time		$V_{GEN}=-10V, R_G=6\Omega$	$t_{d(off)}$	-	42.0	
Turn off Fall Time	$t_f$		-	5.5	-	
<b>Drain-Source Body Diode</b>						
Diode Forward Voltage	$V_{GS}=0V, I_S=-1A$	$V_{SD}$	-	-0.8	-1.3	V
Reverse Recovery Time	$I_{SD}=-3A, di_{SD}/dt=100A/\mu s$	$t_{rr}$	-	7.2	-	ns
Reverse Recovery Charge		$Q_{rr}$	-	2.3	-	nC
Body Diode Continuous Current	-	$I_S$	-	-	1.0	A

Note:

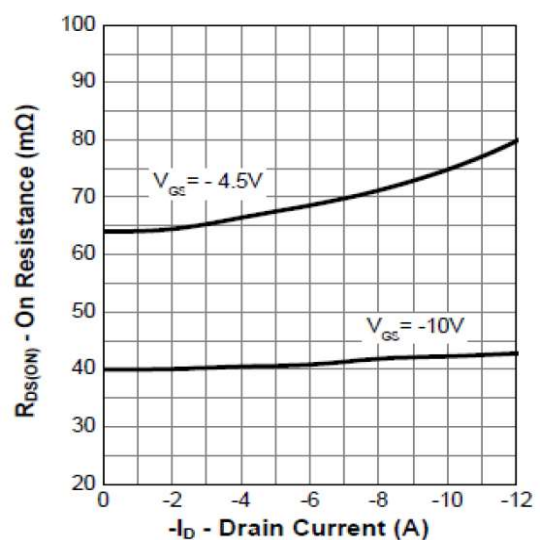
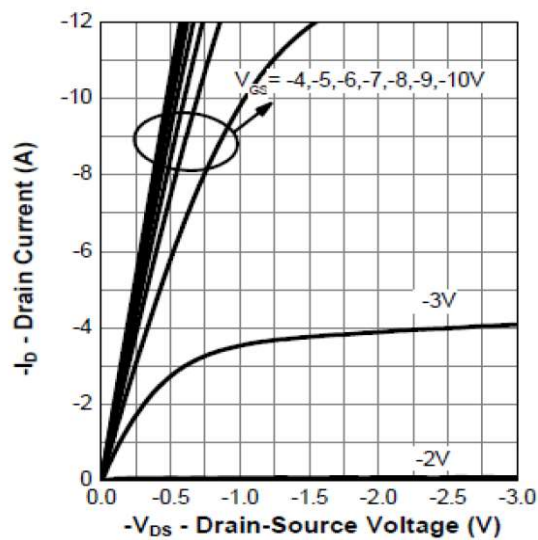
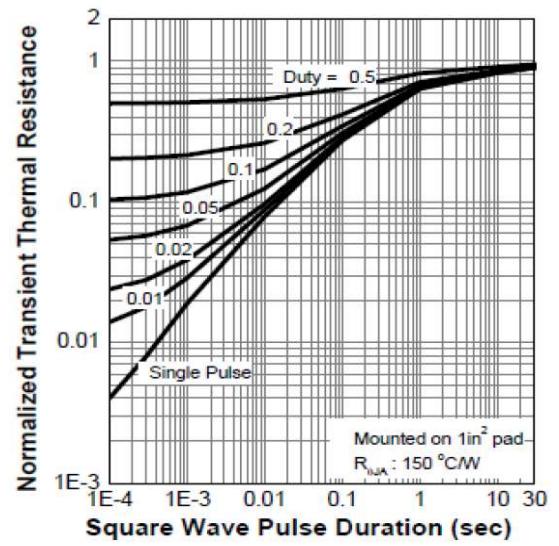
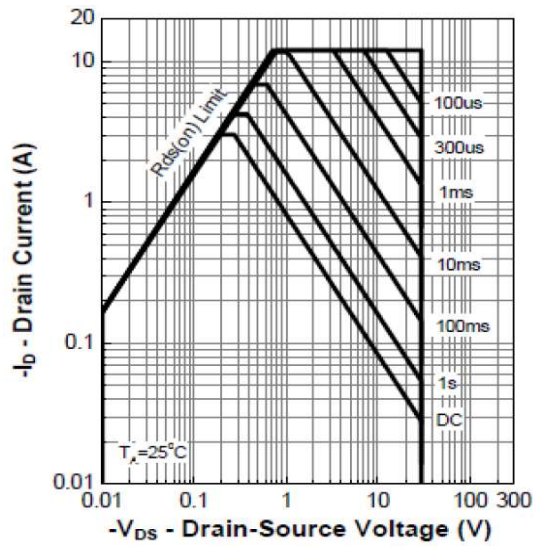
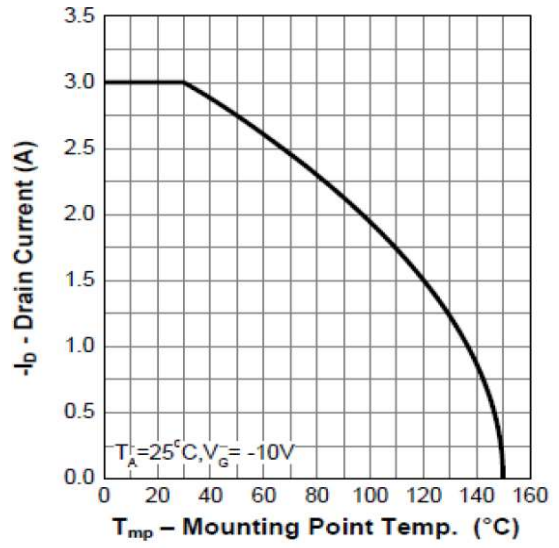
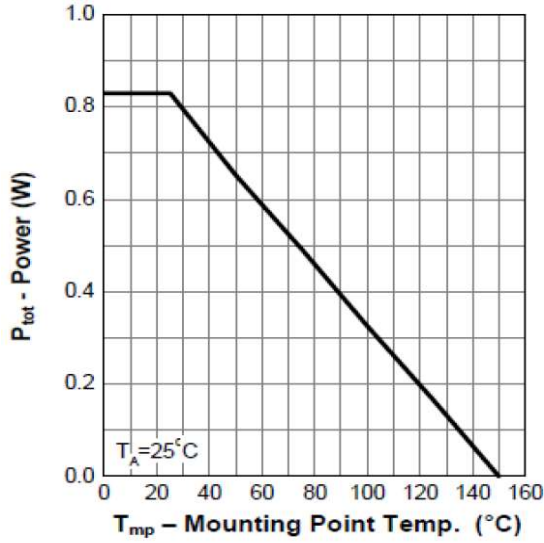
4. Guarantee by design, not test in mass production.



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### RATINGS AND CHARACTERISTIC CURVES



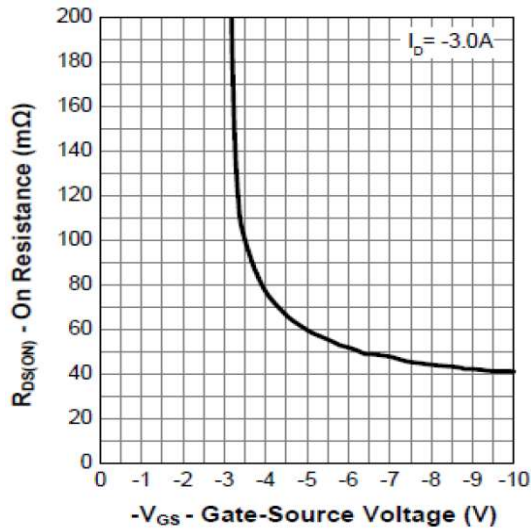


Fig.7 Transfer Characteristics

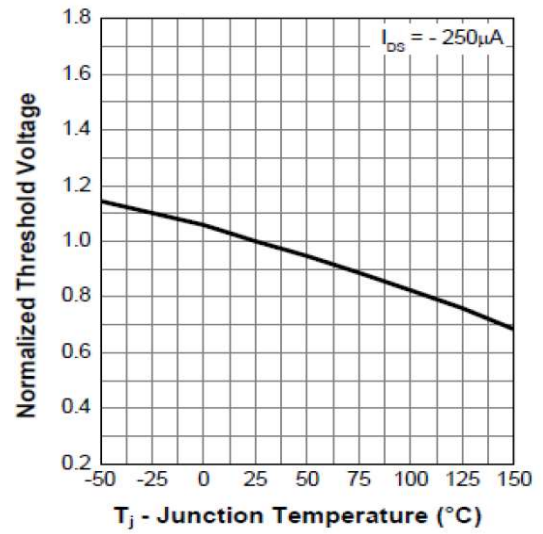


Fig.8 Normalized Threshold Voltage

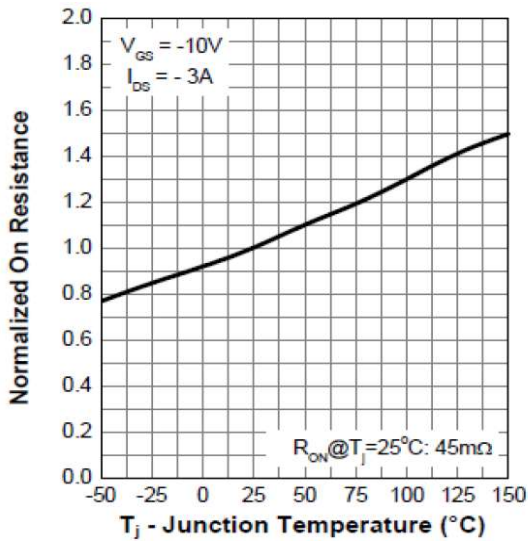


Fig.9 Normalized On Resistance

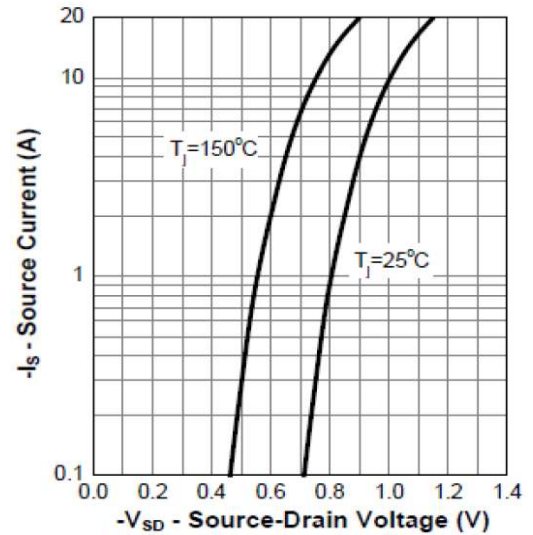


Fig.10 Diode Forward Current

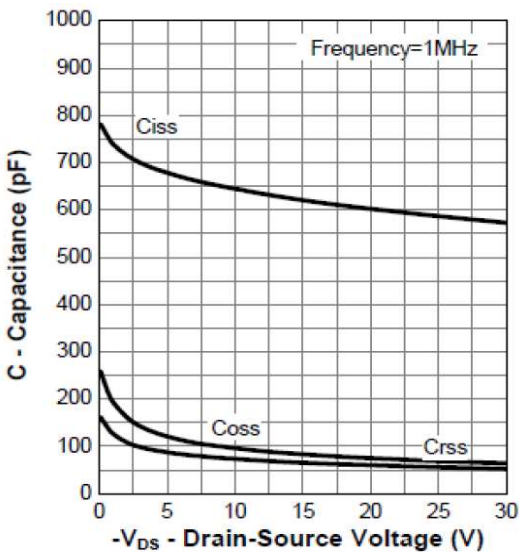


Fig.11 Capacitance

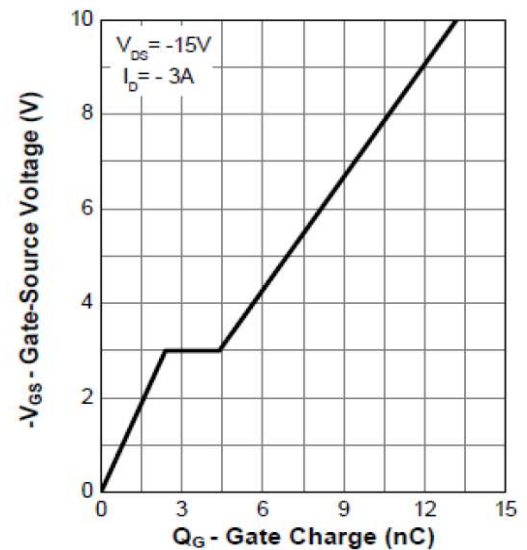


Fig.12 Gate Charge

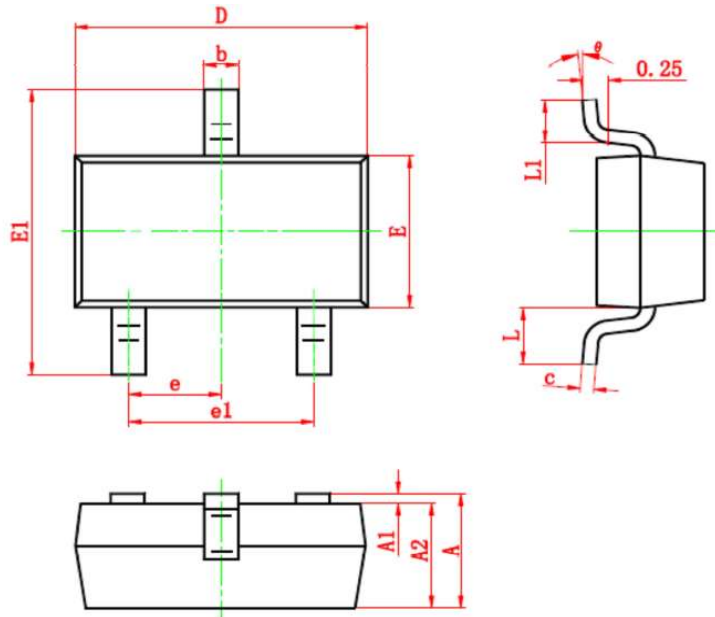


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### Package Dimension

### SOT-23



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.15	0.035	0.045
A1	0.00	0.10	0.000	0.004
A2	0.90	1.05	0.035	0.041
b	0.30	0.50	0.012	0.020
c	0.08	0.15	0.003	0.006
D	2.80	3.00	0.110	0.118
E	1.20	1.40	0.047	0.055
E1	2.25	2.55	0.089	0.100
e	TYP 0.95		TYP 0.037	
e1	1.80	2.00	0.071	0.079
L	REF 0.55		REF 0.022	
L1	0.30	0.50	0.012	0.020
$\theta$	0°	8°	0°	8°