

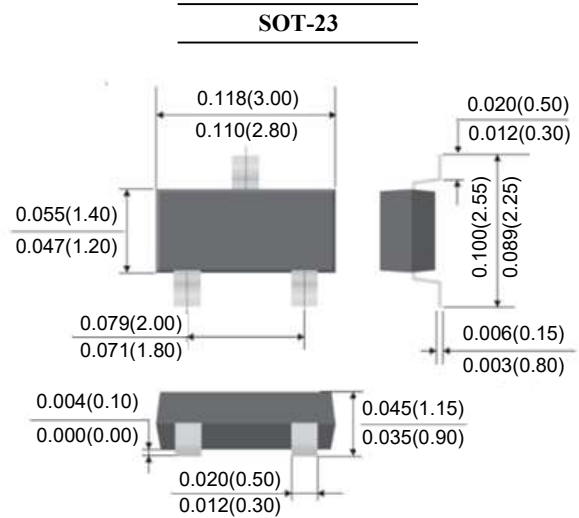
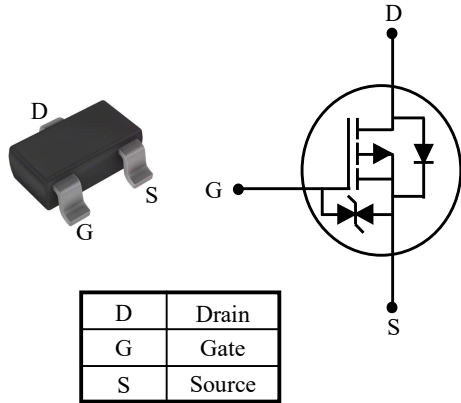


# SM3415KIDSH

## P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- $R_{DS(ON)}=39m\Omega@V_{GS}=-4.5V$
- Low gate charge
- ESD protected gate
- Suffix "H" indicates Halogen-free parts, ex. SM3415KIDSH



### Maximum Ratings(Note 1)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	$V_{DS}$	-20	V	
Gate-Source Voltage	$V_{GS}$	$\pm 8$		
Continuous Drain Current (Note 2)	$I_D$	$T_A=25^\circ C$	-4.2	A
		$T_A=70^\circ C$	-3.3	
Pulsed Drain Current (Note 3)	$I_{DM}$	-10.5	A	
Power Dissipation (Note 4)	$P_D$	$T_A=25^\circ C$	1.00	W
		$T_C=25^\circ C$	1.56	
Thermal Maximum Junction to Ambient (Note 3)	$R_{\theta JA}$	125	$^\circ C/W$	
Thermal Maximum Junction to Case	$R_{\theta JC}$	80	$^\circ C/W$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ C$	

Note:

1.  $T_A=25^\circ C$ . Exposure to absolute maximum rating conditions for extended periods may remain possibility to affect device reliability
2. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
3. The data tested by pulsed , pulse width  $\leq 300\mu s$  , duty cycle  $\leq 2\%$
4. Power dissipation is limited by 150 $^\circ C$  junction temperature.



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### Electrical Characteristics ( $T_A=25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	$V_{(BR)DSS}$	-20	-	-	V
Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	$V_{GS(th)}$	-0.30	-0.55	-0.90	V
Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 8V$	$I_{GSS}$	-	-	$\pm 10$	$\mu A$
Zero Gate Voltage Drain Current	$V_{DS}=-16V, V_{GS}=0V$	$I_{DSS}$	-	-	-1	$\mu A$
Drain-Source On-Resistance	$V_{GS}=-4.5V, I_D=-4.0A$	$R_{DS(on)}$	-	32	39	m $\Omega$
	$V_{GS}=-2.5V, I_D=-4.0A$		-	39	51	
	$V_{GS}=-1.8V, I_D=-2.0A$		-	50	64	
Diode Forward Voltage (Note 3)	$V_{GS}=0V, I_S=-1A$	$V_{SD}$	-	-0.85	-1.10	V
Forward Transconductance	$V_{DS}=-5V, I_D=-4A$	$g_{FS}$	-	11	-	S
<b>Dynamic (Note 5)</b>						
Total Gate Charge	$V_{DS}=-10V, V_{GS}=-2.5V, I_D=-4A$	$Q_g$	-	5.1	-	nC
			-	6.8	-	
			-	1.9	-	
Gate-Source Charge	$V_{DS}=-10V, V_{GS}=-4.5V, I_D=-4A$	$Q_{gs}$	-	1.9	-	nC
Gate-Drain Charge		$Q_{gd}$	-	2.2	-	
Input Capacitance	$V_{DS}=-10V, V_{GS}=0V, f=1MHz$	$C_{iss}$	-	1029	-	pF
Output Capacitance		$C_{oss}$	-	102	-	
Reverse Transfer Capacitance		$C_{rss}$	-	79	-	
Turn on Delay Time	$V_{DS}=-10V, R_{GEN}=3\Omega$ $I_D=-4A, V_{GS}=-4.5V$	$t_{d(on)}$	-	10	-	ns
Turn on Rise Time		$t_r$	-	30	-	
Turn off Delay Time		$t_{d(off)}$	-	55	-	
Turn off Fall Time		$t_f$	-	15	-	

Note:

5. Guarantee by design, not test in mass production



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### RATINGS AND CHARACTERISTIC CURVES

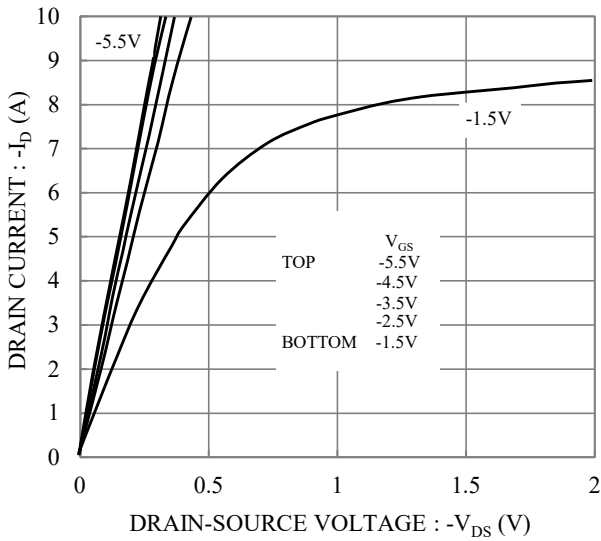


Fig.1 Typical Output Characteristics

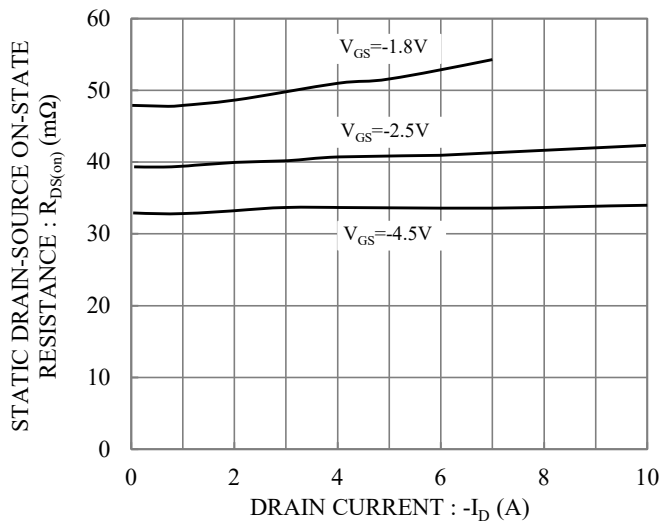


Fig.2 Static Drain-Source On-State Resistance vs. Drain Current

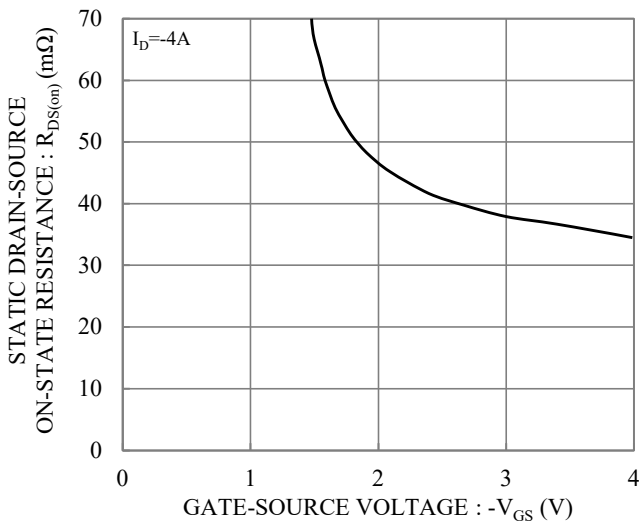


Fig.3 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

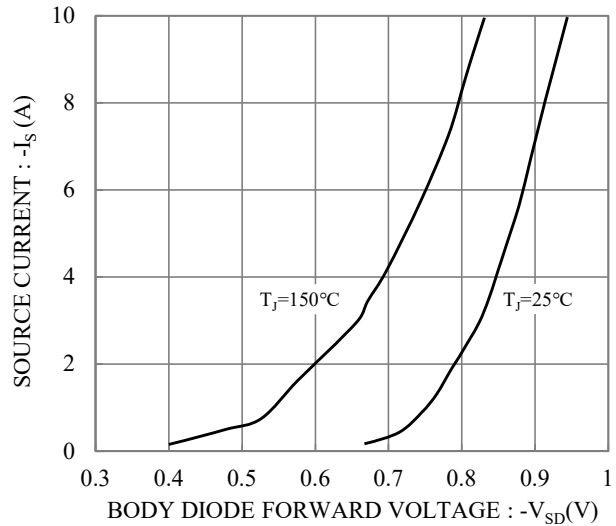


Fig.4 Body Diode Forward Voltage vs. Source Current

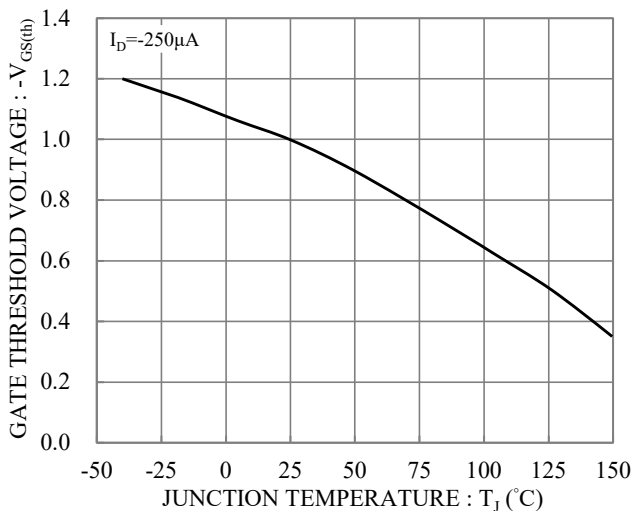


Fig.5 Gate Threshold Voltage vs. Junction Temperature

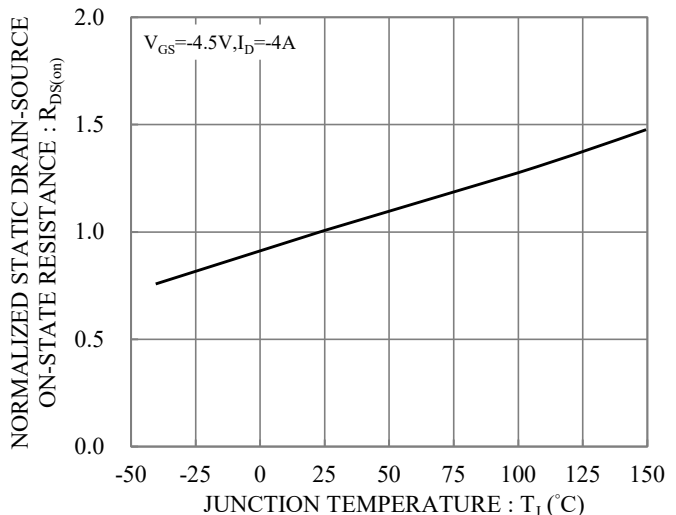
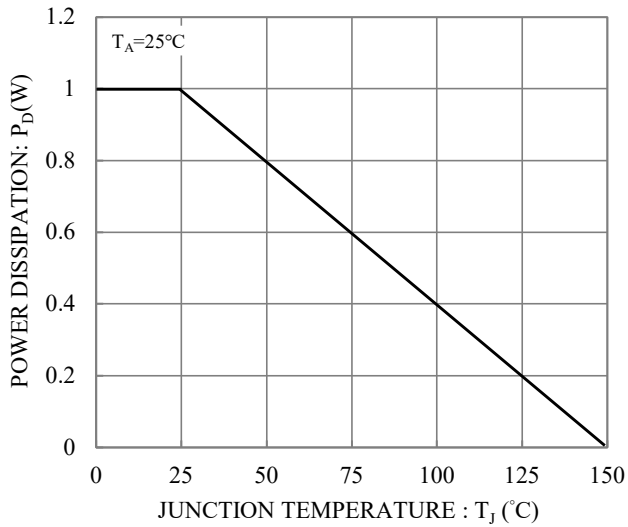


Fig.6 Drain-Source On-State Resistance vs. Junction Temperature

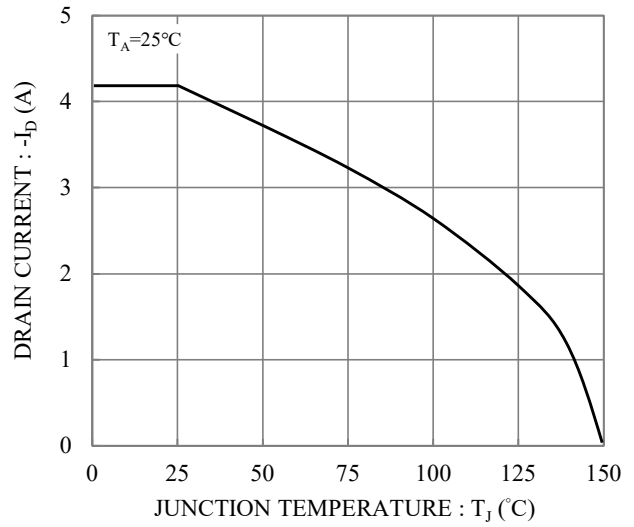


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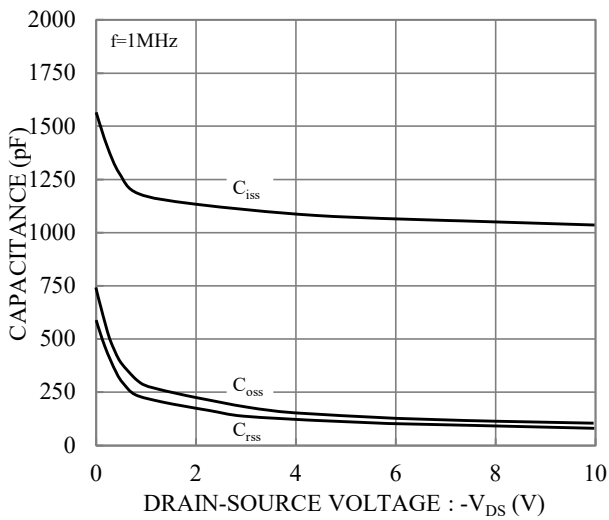
## P-Channel Enhancement Mode Field Effect Transistor



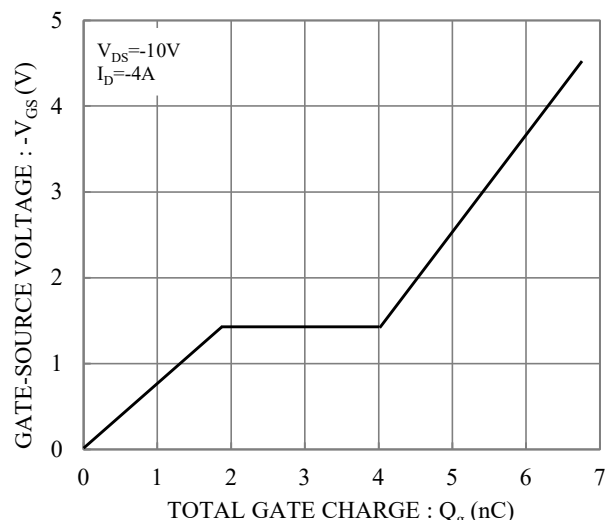
**Fig.7 Power Dissipation**



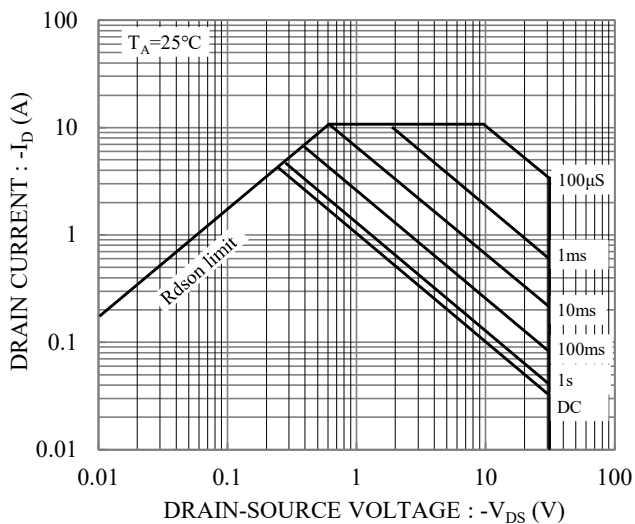
**Fig.8 Drain Current**



**Fig.9 Capacitance vs Drain-Source Voltage**



**Fig.10 Gate Charge**



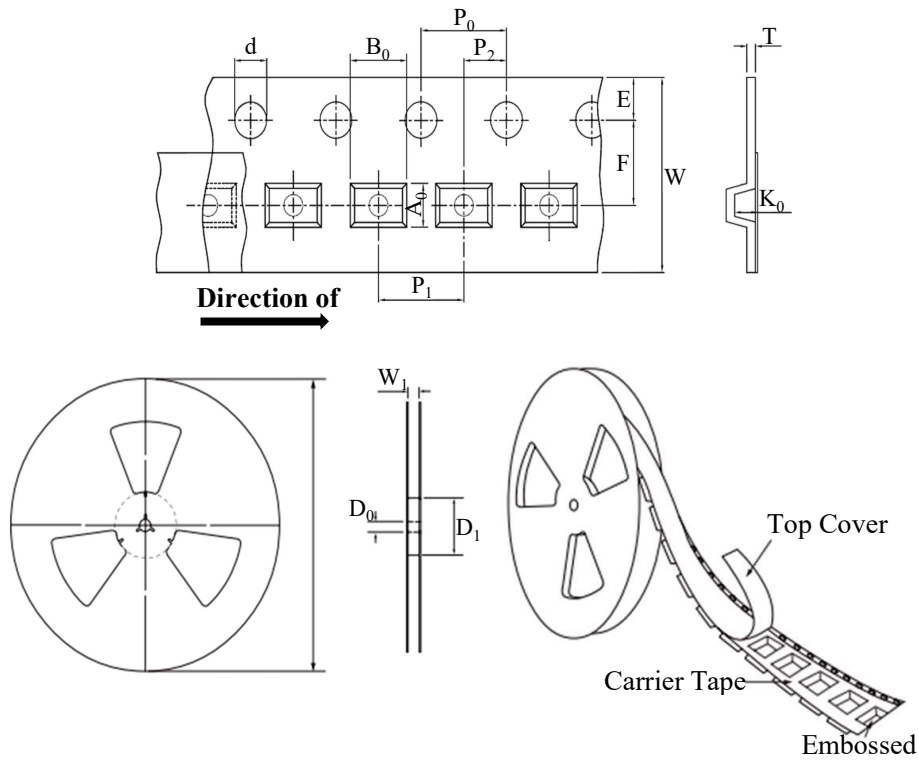
**Fig.11 Safe Operating Area**



# SM3415KIDSH

## P-Channel Enhancement Mode Field Effect Transistor

### TAPE & REEL SPECIFICATION



Item	Symbol	SOT-23
Carrier width	A <sub>0</sub>	3.30 ± 0.10
Carrier length	B <sub>0</sub>	3.00 ± 0.10
Carrier depth	K <sub>0</sub>	1.70 ± 0.10
Sprocket hole	d	1.50 ± 0.10
Reel outside diameter	D	178.00 ± 2.00
Feed hole width	D <sub>0</sub>	13.00 ± 0.50
Reel inner diameter	D <sub>1</sub>	MIN. 50.00
Sprocket hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.10
Sprocket hole pitch	P <sub>0</sub>	4.00 ± 0.10
Punch hole pitch	P <sub>1</sub>	4.00 ± 0.10
Embossment center	P <sub>2</sub>	2.00 ± 0.10
Overall tape thickness	T	0.20 ± 0.05
Tape width	W	8.00 ± 0.20
Reel width	W <sub>1</sub>	MAX. 14.50

### MARKING CODE

Part Number	Marking Code
SM3415KIDSH	NM□□
	01□□

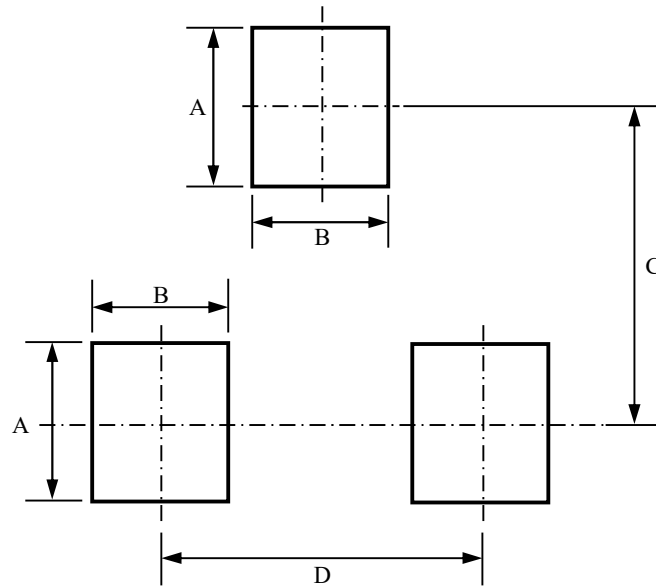
□□ =====> Date Code



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*P-Channel Enhancement Mode Field Effect Transistor*

## SUGGESTED SOLDER PAD LAYOUT



Unit :mm

PACKAGE	A	B	C	D
SOT-23	0.80	0.60	2.02	1.90