

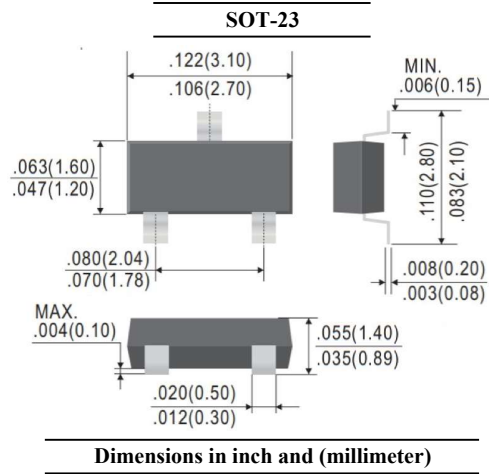
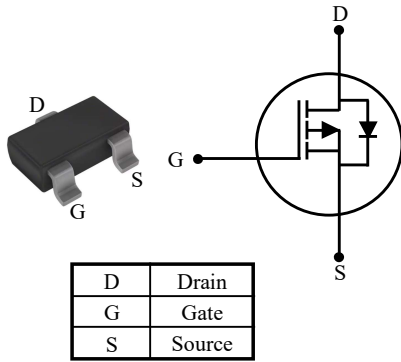


# SM06P5K4TDSH

## P-Channel Enhancement Mode Field Effect Transistor

### FEATURES

· Suffix "H" indicates Halogen-free parts, ex.SM06P5K4TDSH



### Maximum Ratings ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-60	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current	$I_D$	-0.4	A
Pulsed Drain Current (Note 1)	$I_{DM}$	-1.2	A
Power Dissipation (Note 2)	$P_D$	0.5	W
Thermal Resistance from Junction to Ambient (Note 2)	$R_{\theta JA}$	250	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$

Note :

1. Pulse Width  $\leq 100\mu\text{s}$ , Duty Cycle  $\leq 2\%$ , Repetitive rating, pulse width limited by junction temperature  $T_{J(\text{MAX})} = 150^\circ\text{C}$ .
2. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.



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### Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain Source Breakdown Voltage	$I_D = -250\mu\text{A}$	$V_{(BR)DSS}$	-60	-	-	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	$V_{GS(th)}$	-0.8	-	-2.0	V
Zero Gate Voltage Drain Current	$V_{DS} = -60\text{V}$	$I_{DSS}$	-	-	-1	$\mu\text{A}$
Gate-Body Leakage Current	$V_{GS} = \pm 20\text{V}$	$I_{GSS}$	-	-	$\pm 0.1$	$\mu\text{A}$
Drain-Source On-State Resistance	$V_{GS} = -10\text{V}, I_D = -0.2\text{A}$	$R_{DS(on)}$	-	-	3.6	$\Omega$
	$V_{GS} = -4.5\text{V}, I_D = -0.1\text{A}$		-	-	5.4	
Forward Transconductance	$V_{DS} = -5\text{V}, I_D = -0.2\text{A}$	$g_{FS}$	-	0.4	-	S
<b>Dynamic</b>						
Total Gate Charge	$V_{DS} = -30\text{V}, V_{GS} = -10\text{V}, I_D = -0.4\text{A}$	$Q_g$	-	0.9	-	nC
			-	1.7	-	
			-	-	-	
Gate-Source Charge	$V_{DS} = -30\text{V}, V_{GS} = -4.5\text{V}, I_D = -0.4\text{A}$	$Q_{gs}$	-	0.5	-	nC
Gate-Drain Charge		$Q_{gd}$	-	0.2	-	
Input Capacitance	$V_{DS} = -30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	$C_{iss}$	-	42.0	-	pF
Output Capacitance		$C_{oss}$	-	3.6	-	
Reverse Transfer Capacitance		$C_{rss}$	-	1.4	-	
Turn-On Delay Time	$V_{DS} = -30\text{V}, I_D = -0.4\text{A},$ $V_{GS} = -10\text{V}, R_g = 3.9\Omega$	$t_{d(on)}$	-	6.8	-	ns
Turn-On Rise Time		$t_r$	-	7.5	-	
Turn-Off Delay Time		$t_{d(off)}$	-	36.0	-	
Turn-Off Fall Time		$t_f$	-	22.0	-	
<b>Drain-Source Body Diode</b>						
Drain-Source Diode Forward Voltage	$I_S = -0.1\text{A}, V_{GS} = 0\text{V}$	$V_{SD}$	-	-	-1	V
Diode Continuous Forward Current	-	$I_S$	-	-	-0.4	A
Reverse Recovery Time	$I_S = -0.4\text{A}, di/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	-	20	-	ns
Reverse Recovery Charge		$Q_{rr}$	-	13	-	nC



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### RATINGS AND CHARACTERISTIC CURVES

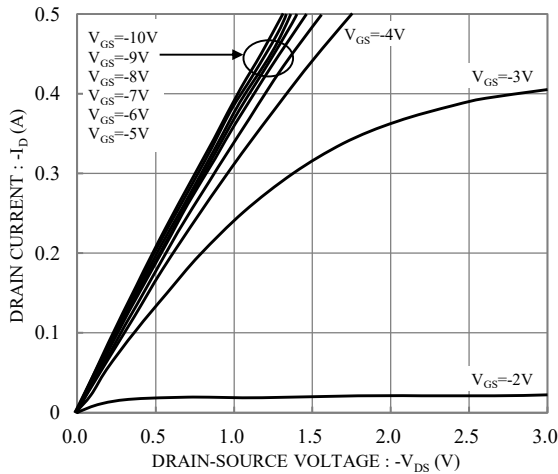


Fig.1 Typical Output Characteristics

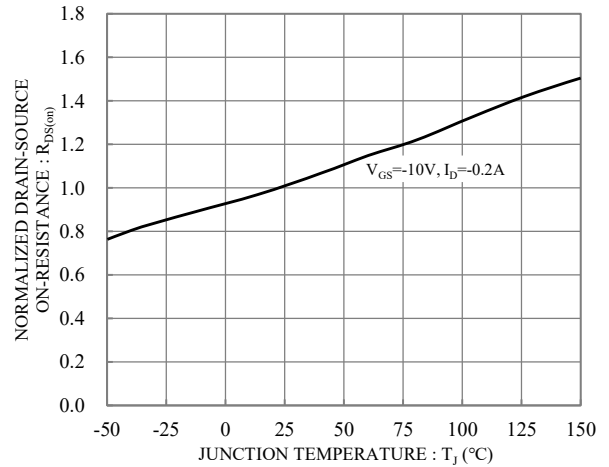


Fig.2 On-Resistance vs. Junction Temperature

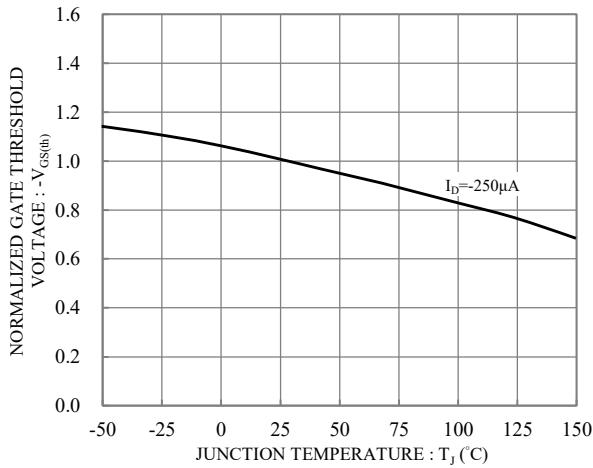


Fig.3 Gate Threshold Voltage vs. Junction Temperature

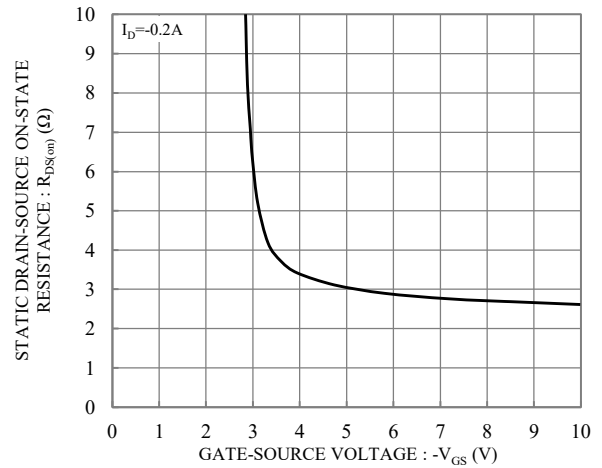


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

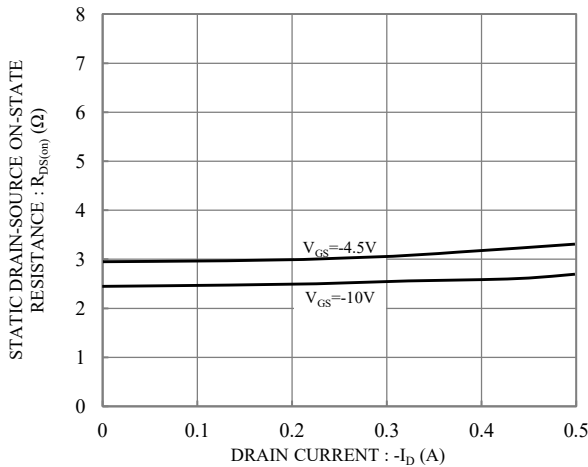


Fig.5 Static Drain-Source On-State Resistance vs. Drain current

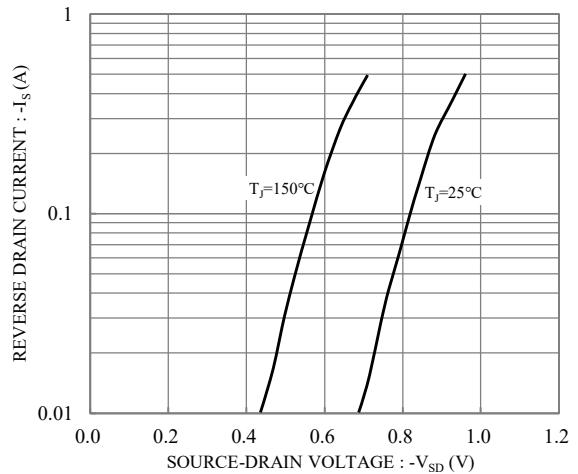
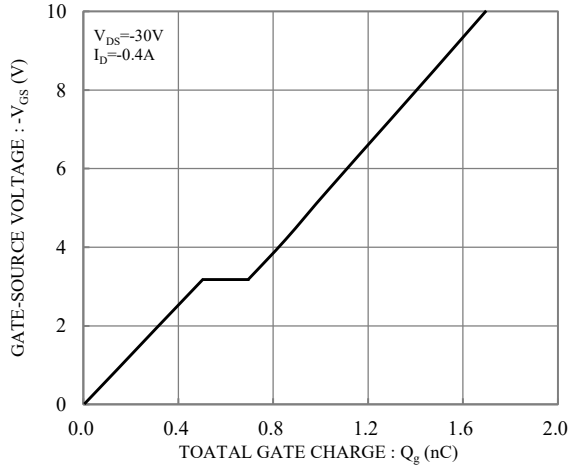


Fig.6 Typical Forward Characteristic

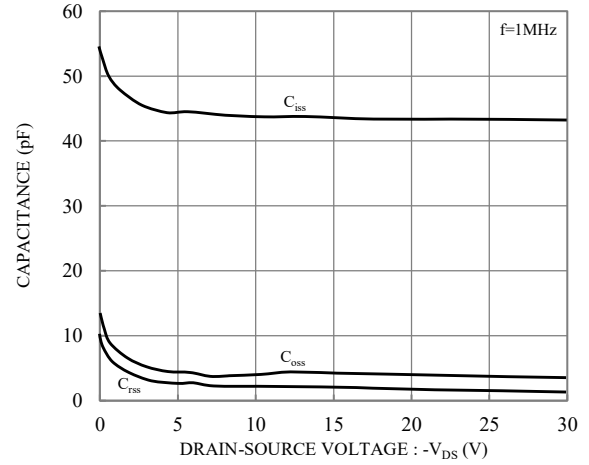


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## P-Channel Enhancement Mode Field Effect Transistor



**Fig.7 Gate Charge**



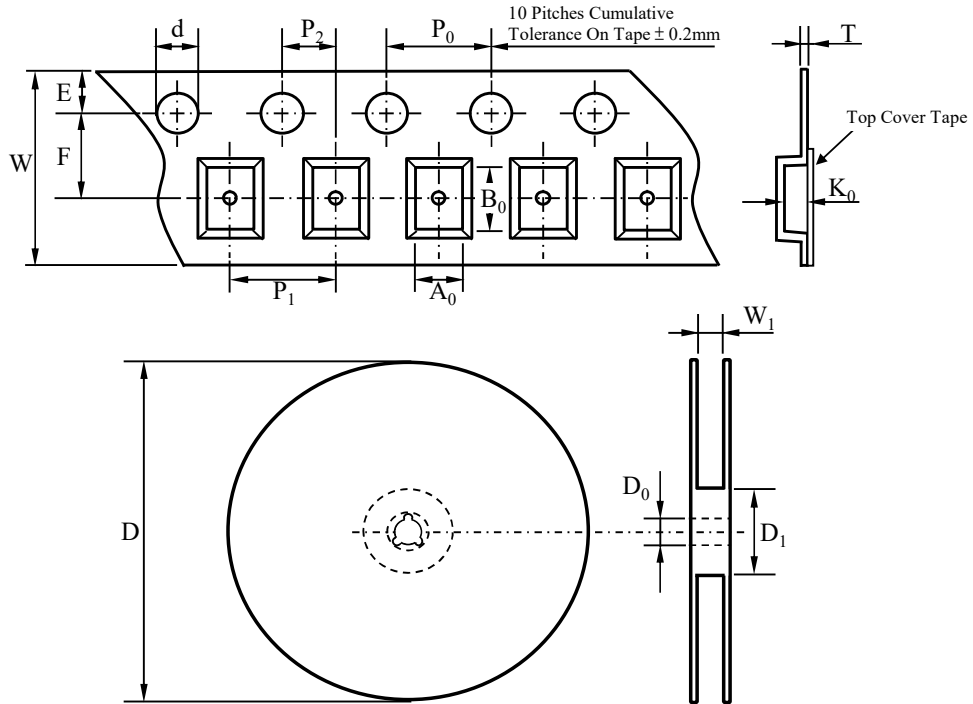
**Fig.8 Capacitance vs. Drain-Source Voltage**



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## P-Channel Enhancement Mode Field Effect Transistor

### TAPE & REEL SPECIFICATION



Item	Symbol	SOT-23
Carrier width	A <sub>0</sub>	*
Carrier length	B <sub>0</sub>	
Carrier depth	K <sub>0</sub>	
Sprocket hole	d	1.60 ± 0.10
Reel outside diameter	D	178.00 ± 2.00
Feed hole width	D <sub>0</sub>	13.00 ± 0.50
Reel inner diameter	D <sub>1</sub>	MIN. 50.00
Sprocket hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.10
Sprocket hole pitch	P <sub>0</sub>	4.00 ± 0.10
Punch hole pitch	P <sub>1</sub>	4.00 ± 0.10
Embossment center	P <sub>2</sub>	2.00 ± 0.10
Overall tape thickness	T	0.20 ± 0.05
Tape width	W	8.00 ± 0.20
Reel width	W <sub>1</sub>	MAX. 14.50

Note \*: A<sub>0</sub>, B<sub>0</sub>, and K<sub>0</sub> are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max.

### ORDER INFORMATION

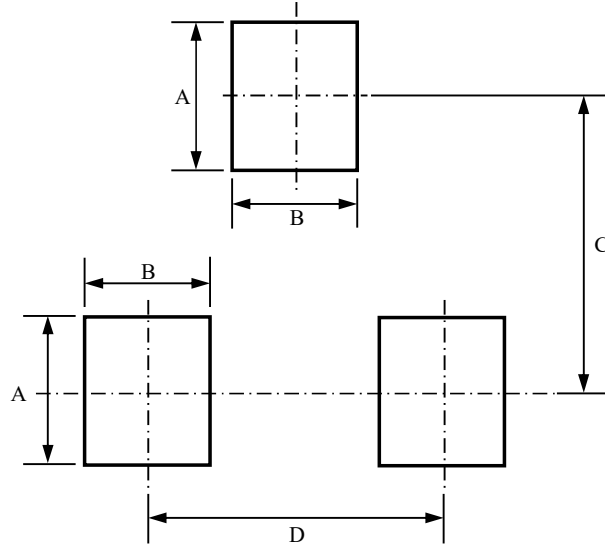
Part Number	Marking Code	Reel Size	Quantity
SM06P5K4TDSH	PA1	7"	3,000



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*P-Channel Enhancement Mode Field Effect Transistor*

## **SUGGESTED SOLDER PAD LAYOUT**



**Unit :mm**

PACKAGE	A	B	C	D
SOT-23	1.00	0.80	2.00	1.90