

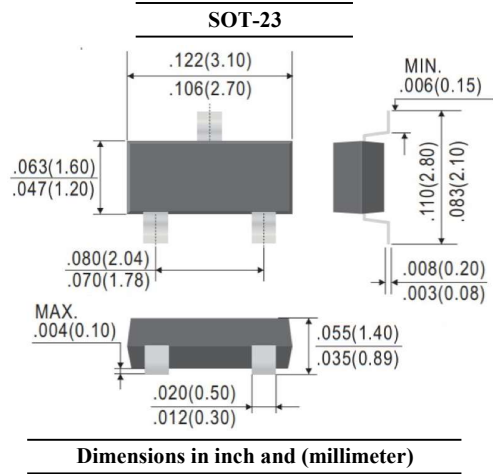
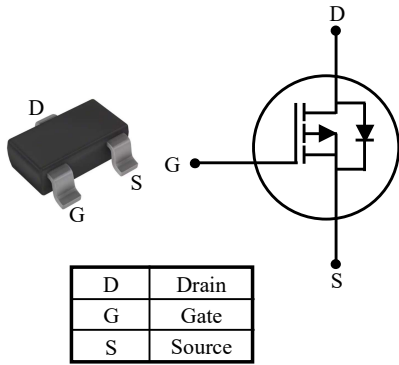


SM03P072TDSH

P-Channel Enhancement Mode Field Effect Transistor

FEATURES

- Suffix "H" indicates Halogen-free parts, ex.SM03P072TDSH



Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 12	V
Drain Current	I_D	-4	A
Pulsed Drain Current (Note 1)	I_{DM}	-27	A
Power Dissipation (Note 2)	P_D	1.4	W
Thermal Resistance from Junction to Ambient (Note 2)	$R_{\theta JA}$	90	$^\circ\text{C}/\text{W}$
Operating and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$

Note :

1. Pulse Width $\leq 100\mu\text{s}$, Duty Cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)} = 150^\circ\text{C}$.
2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate, at $t \leq 10\text{s}$.



SM03P072TDSH

P-Channel Enhancement Mode Field Effect Transistor

Electrical Characteristics ($T_A=25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static						
Drain Source Breakdown Voltage	$I_D=-250\mu\text{A}$	$V_{(BR)DSS}$	-30	-	-	V
Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	$V_{GS(th)}$	-0.7	-	-1.3	V
Zero Gate Voltage Drain Current	$V_{DS}=-30\text{V}$	I_{DSS}	-	-	-1	μA
Gate-Body Leakage Current	$V_{GS}=\pm 12\text{V}$	I_{GSS}	-	-	± 0.1	μA
Drain-Source On-State Resistance	$V_{GS}=-10\text{V}, I_D=-4\text{A}$	$R_{DS(on)}$	-	-	54	m Ω
	$V_{GS}=-4.5\text{V}, I_D=-3.7\text{A}$		-	-	72	
	$V_{GS}=-2.5\text{V}, I_D=-2\text{A}$		-	-	120	
Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-3\text{A}$	g_{FS}	-	8.6	-	S
Dynamic						
Gate Resistance	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	R_g	-	10.9	-	Ω
Total Gate Charge	$V_{GS}=-2.5\text{V}, V_{DS}=-15\text{V}, I_D=-3\text{A}$	Q_g	-	4.0	-	nC
			-	6.6	-	
Gate-Source Charge	$V_{GS}=-4.5\text{V}, V_{DS}=-15\text{V}, I_D=-3\text{A}$	Q_{gs}	-	1.0	-	
Gate-Drain Charge		Q_{gd}	-	2.4	-	
Input Capacitance	$V_{DS}=-15\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	C_{iss}	-	454	-	pF
Output Capacitance		C_{oss}	-	68	-	
Reverse Transfer Capacitance		C_{rss}	-	64	-	
Turn-On Delay Time	$V_{DS}=-15\text{V}, I_D=-3\text{A},$ $V_{GS}=-4.5\text{V}, R_g=3.3\Omega$	$t_{d(on)}$	-	11.0	-	ns
Turn-On Rise Time		t_r	-	28.0	-	
Turn-Off Delay Time		$t_{d(off)}$	-	20.0	-	
Turn-Off Fall Time		t_f	-	6.0	-	
Drain-Source Body Diode						
Drain-Source Diode Forward Voltage	$I_S=-4\text{A}, V_{GS}=0\text{V}$	V_{SD}	-	-	-1.3	V
Diode Continuous Forward Current	-	I_S	-	-	-4	A
Reverse Recovery Time	$I_S=-3\text{A}, di/dt=100\text{A}/\mu\text{s}$	t_{rr}	-	8	-	ns
Reverse Recovery Charge		Q_{rr}	-	3.4	-	nC



SM03P072TDSH

P-Channel Enhancement Mode Field Effect Transistor

RATINGS AND CHARACTERISTIC CURVES

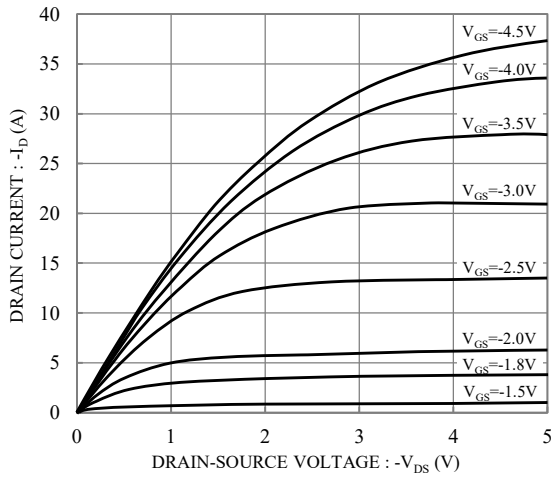


Fig.1 Typical Output Characteristics

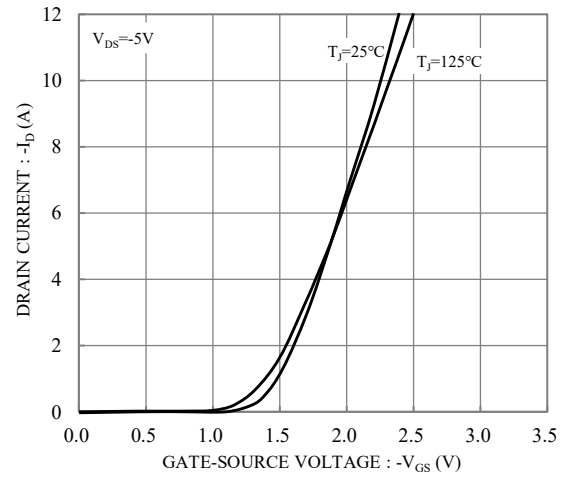


Fig.2 Typical Transfer Characteristics

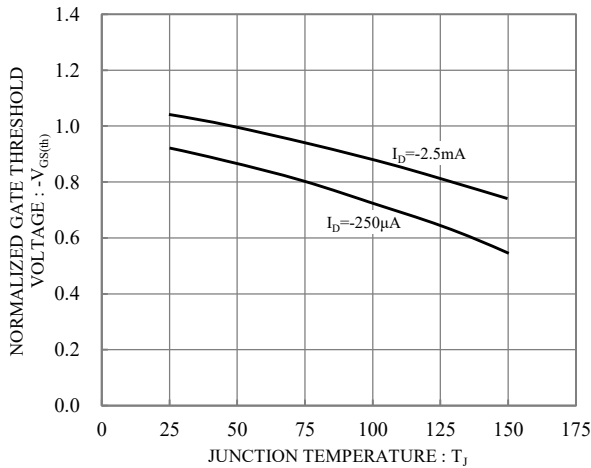


Fig.3 Gate Threshold Voltage vs. Junction Temperature

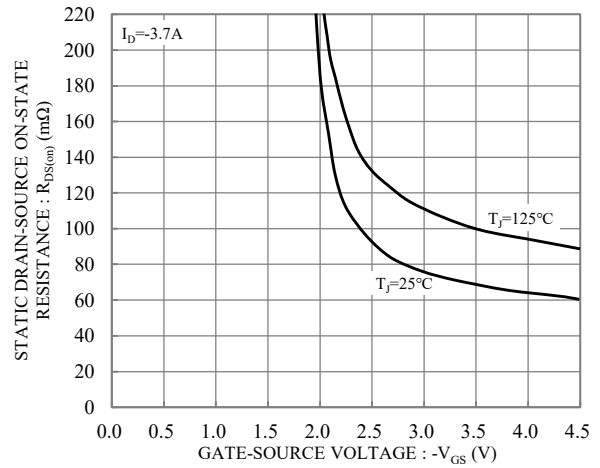


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

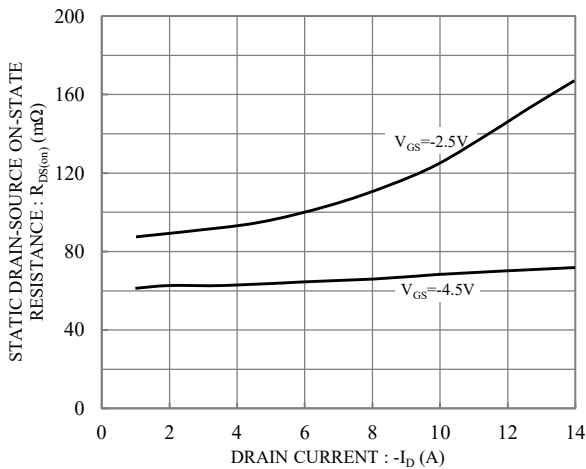


Fig.5 Static Drain-Source On-State Resistance vs. Drain current

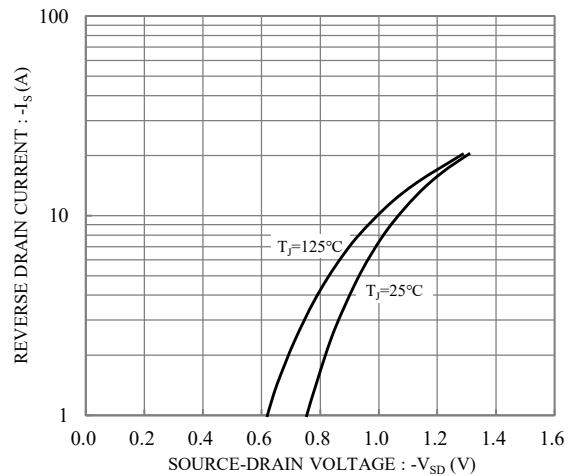


Fig.6 Typical Forward Characteristic



SM03P072TDSH

P-Channel Enhancement Mode Field Effect Transistor

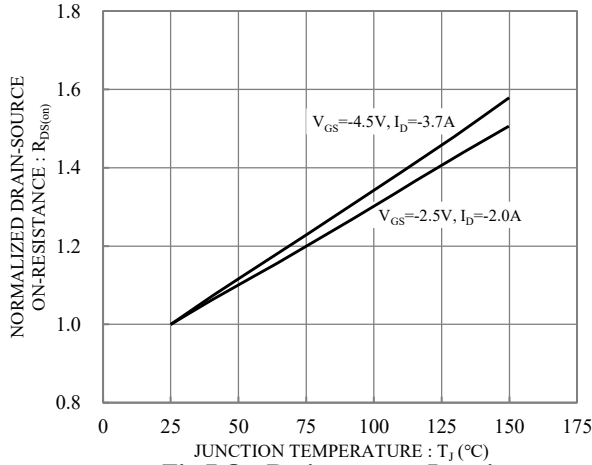


Fig.7 On-Resistance vs. Junction Temperature

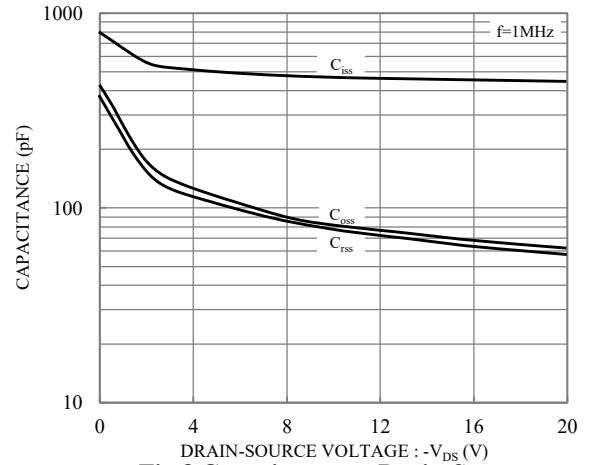


Fig.8 Capacitance vs. Drain-Source Voltage

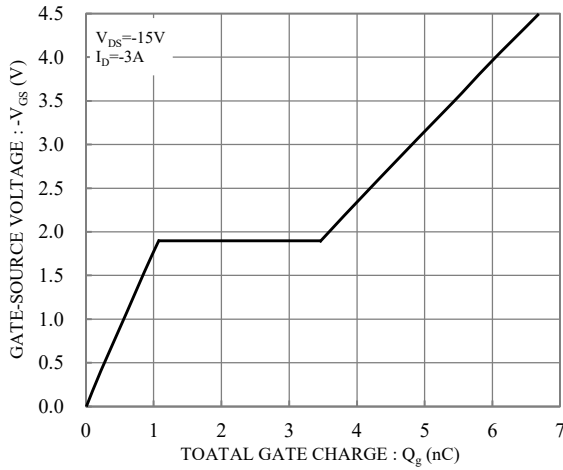


Fig.9 Gate Charge

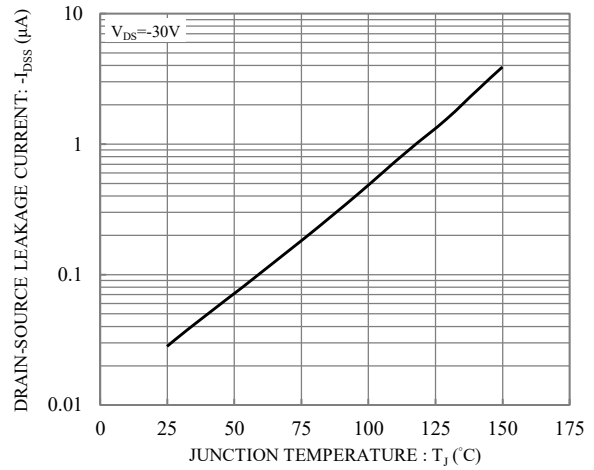


Fig.10 Drain-Source Leakage Current vs. Junction Temperature

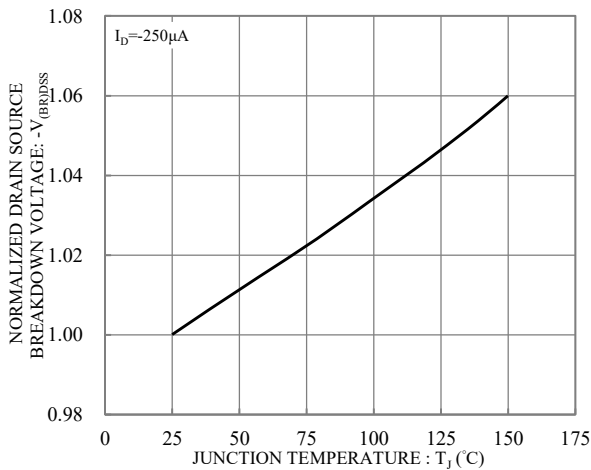


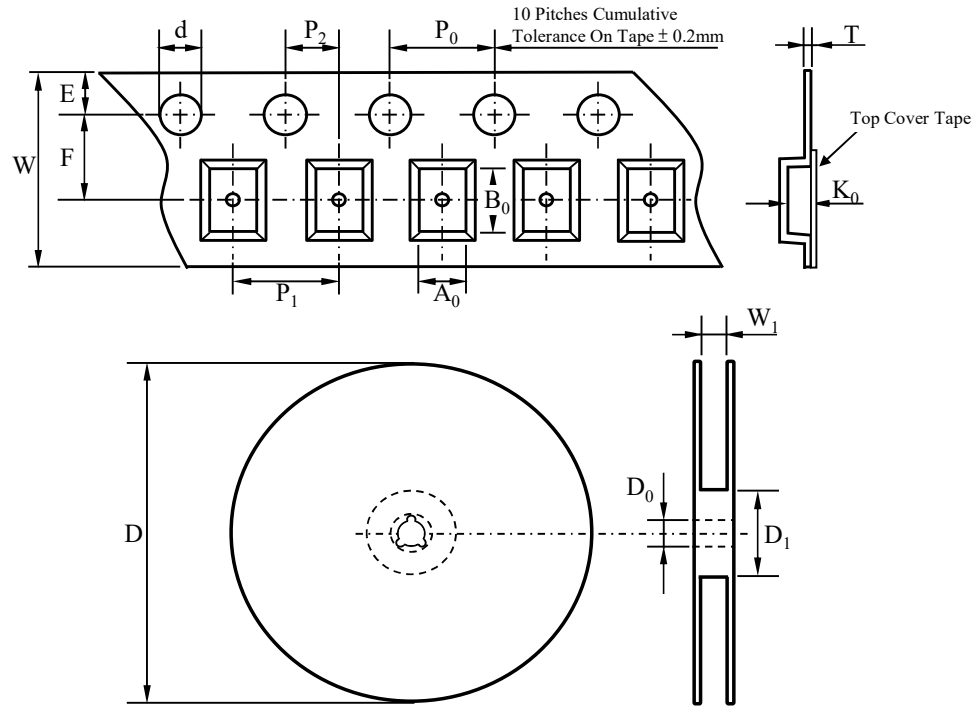
Fig.11 Drain Source Breakdown Voltage vs. Junction Temperature



SM03P072TDSH

P-Channel Enhancement Mode Field Effect Transistor

TAPE & REEL SPECIFICATION



Item	Symbol	SOT-23
Carrier width	A_0	*
Carrier length	B_0	
Carrier depth	K_0	
Sprocket hole	d	1.60 ± 0.10
Reel outside diameter	D	178.00 ± 2.00
Feed hole width	D_0	13.00 ± 0.50
Reel inner diameter	D_1	MIN. 50.00
Sprocket hole position	E	1.75 ± 0.10
Punch hole position	F	3.50 ± 0.10
Sprocket hole pitch	P_0	4.00 ± 0.10
Punch hole pitch	P_1	4.00 ± 0.10
Embossment center	P_2	2.00 ± 0.10
Overall tape thickness	T	0.20 ± 0.05
Tape width	W	8.00 ± 0.20
Reel width	W_1	MAX. 14.50

Note *: A_0 , B_0 , and K_0 are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max.

ORDER INFORMATION

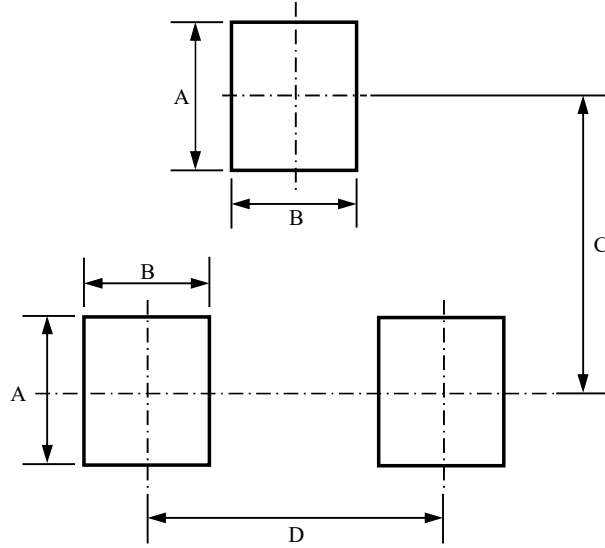
Part Number	Marking Code	Reel Size	Quantity
SM03P072TDSH	LS	7"	3,000



SM03P072TDSH

P-Channel Enhancement Mode Field Effect Transistor

SUGGESTED SOLDER PAD LAYOUT



Unit :mm

PACKAGE	A	B	C	D
SOT-23	1.00	0.80	2.00	1.90