

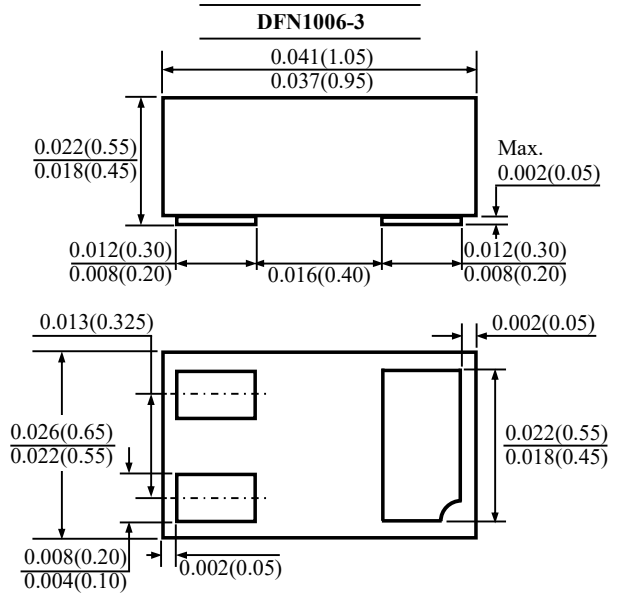
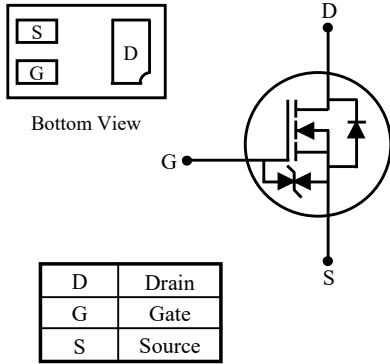


# SM03N650KLPH

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- Low on resistance  $R_{DS(on)}$
- ESD protected gate
- Suffix "H" indicates Halogen-free parts, ex. SM03N650KLPH



### Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DSS}$	30	V
Gate-Source Voltage	$V_{GSS}$	$\pm 12$	V
Drain Current	$I_D$	700	mA
Peak Drain Current, pulsed (Note 1)	$I_{DM}$	3	A
Power Dissipation (Note 2)	$P_D$	690	mW
Thermal Resistance from Junction to Ambient (Note 2)	$R_{\theta JA}$	181	$^\circ\text{C/W}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$

Note :

1. Pulse test: Pulse width  $\leq 100\mu\text{s}$ , Duty cycle  $\leq 2\%$ , Repetitive rating, pulse width limited by junction temperature  $T_{J(MAX)} = 150^\circ\text{C}$ .
2. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.



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### Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain Source Breakdown Voltage	$I_D = 250\mu\text{A}$	$V_{(BR)DSS}$	30	-	-	V
Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$	$I_{DSS}$	-	-	0.1	$\mu\text{A}$
Gate Source Leakage Current	$V_{GS} = \pm 12\text{V}$	$I_{GSS}$	-	-	$\pm 10$	$\mu\text{A}$
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(th)}$	0.5	-	1.5	V
Static Drain Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 700\text{mA}$	$R_{DS(on)}$	-	-	600	m $\Omega$
	$V_{GS} = 4.5\text{V}, I_D = 590\text{mA}$		-	-	650	
	$V_{GS} = 2.5\text{V}, I_D = 590\text{mA}$		-	-	900	
Forward Transconductance	$V_{DS} = 3\text{V}, I_D = 10\text{mA}$	$g_{FS}$	-	100	-	mS
<b>Dynamic</b>						
Gate Resistance	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	$R_g$	-	59	-	$\Omega$
Total Gate Charge	$V_{DS} = 15\text{V}, I_D = 0.5\text{A}, V_{GS} = 4.5\text{V}$	$Q_g$	-	0.70	-	nC
			-	1.72	-	
Gate-Source Charge	$V_{DS} = 15\text{V}, I_D = 0.5\text{A}, V_{GS} = 10\text{V}$	$Q_{gs}$	-	0.35	-	
Gate-Drain Charge		$Q_{gd}$	-	0.17	-	
Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	$C_{iss}$	-	43.0	-	pF
Output Capacitance		$C_{oss}$	-	13.0	-	
Reverse Transfer Capacitance		$C_{rss}$	-	9.5	-	
Turn-On Delay Time	$V_{DS} = 15\text{V}, V_{GS} = 10\text{V}, I_D = 1\text{A}, R_g = 51\Omega$	$t_{d(on)}$	-	10.5	-	ns
Turn-On Rise Time		$t_r$	-	4.8	-	
Turn-Off Delay Time		$t_{d(off)}$	-	10.0	-	
Turn-Off Fall Time		$t_f$	-	7.5	-	
<b>Drain-Source Body Diode</b>						
Diode Forward Voltage	$I_S = 10\text{mA}$	$V_{SD}$	-	0.7	1.2	V
Diode Continuous Forward Current	-	$I_S$	-	-	700	mA
Reverse Recovery Time	$I_S = 1\text{A}, di/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	-	6.3	-	ns
Reverse Recovery Charge		$Q_{rr}$	-	2	-	nC



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### RATINGS AND CHARACTERISTIC CURVES

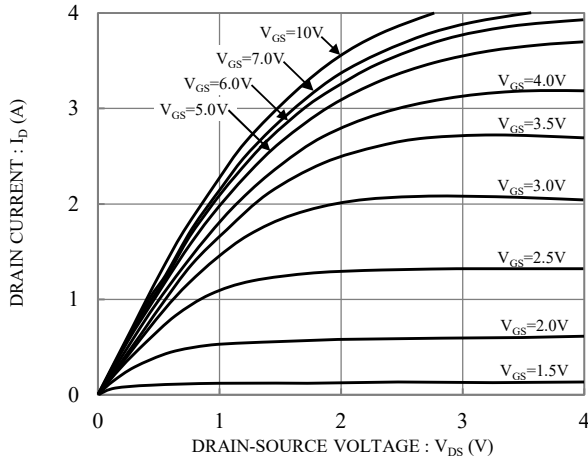


Fig.1 Typical Output Characteristics

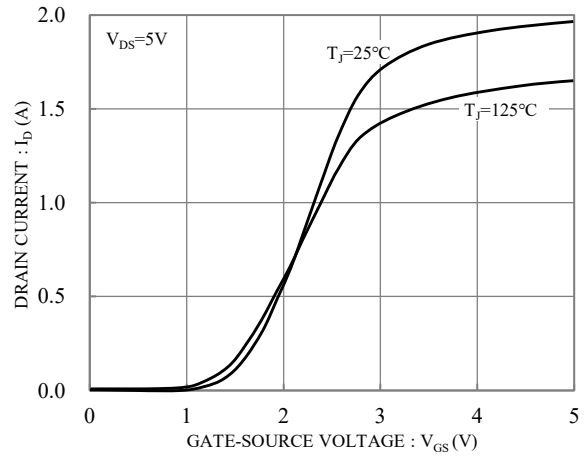


Fig.2 Typical Transfer Characteristics

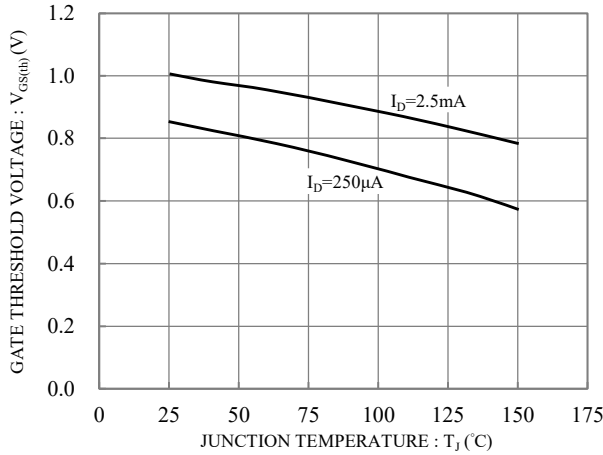


Fig.3 Gate Threshold Voltage vs. Junction Temperature

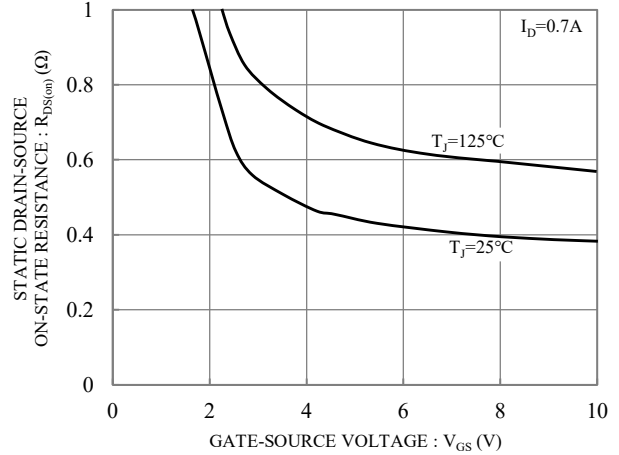


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

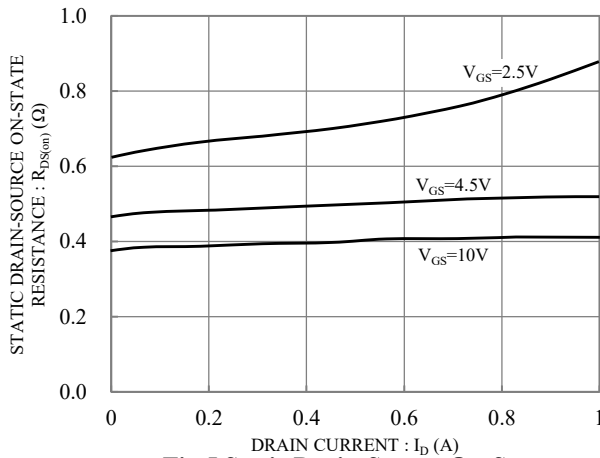


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

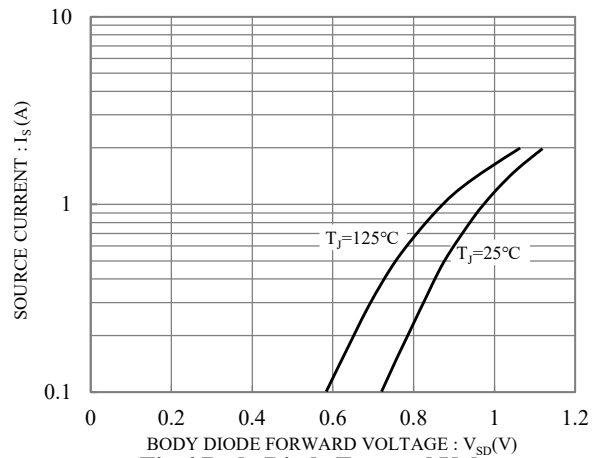
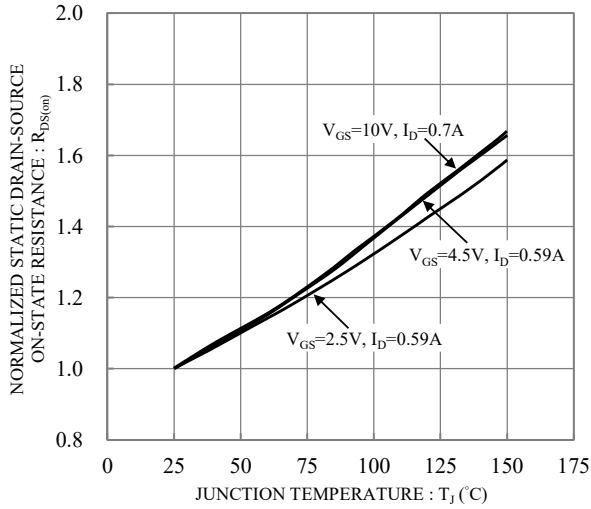


Fig.6 Body Diode Forward Voltage vs. Source Current

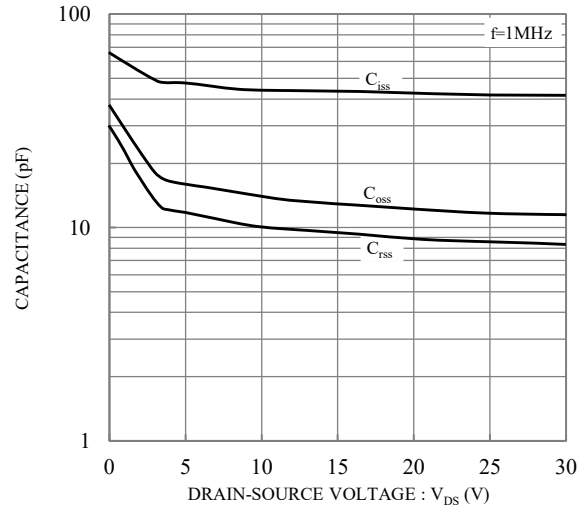


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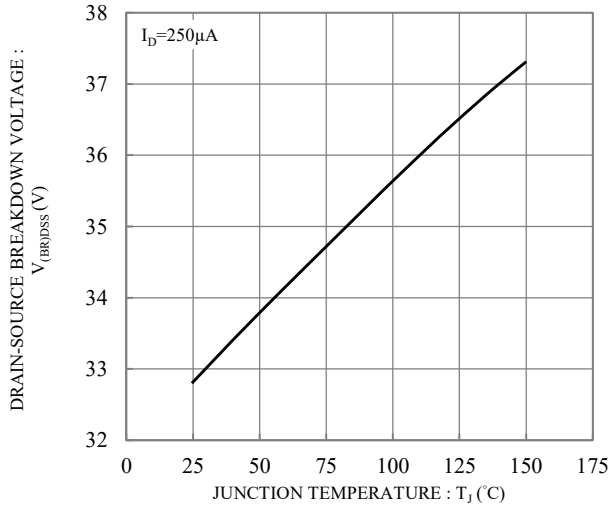
## N-Channel Enhancement Mode Field Effect Transistor



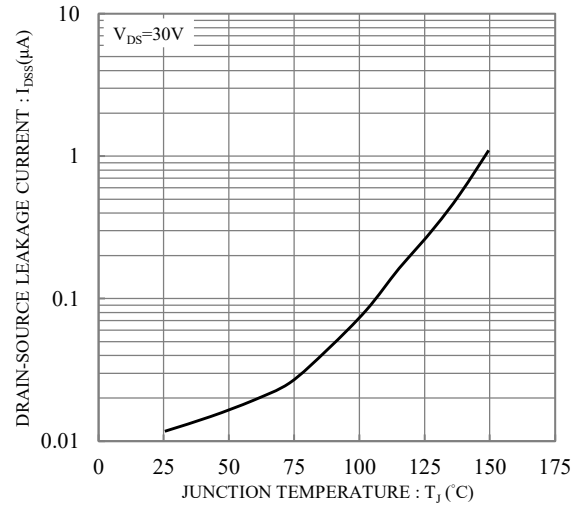
**Fig.7 Drain-Source On-State Resistance vs. Junction Temperature**



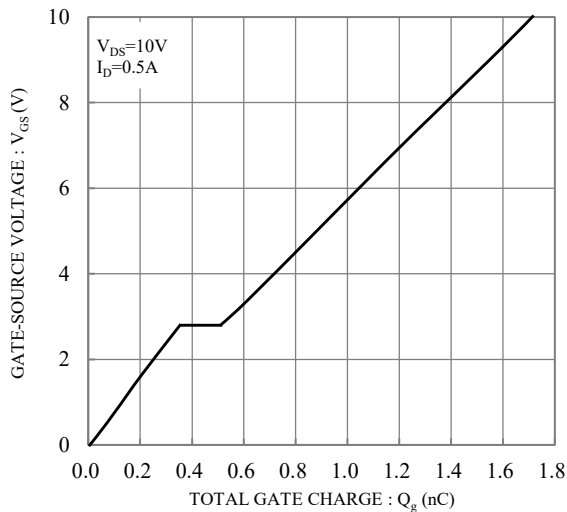
**Fig.8 Capacitance vs. Drain-Source Voltage**



**Fig.9 Breakdown Voltage vs. Junction Temperature**



**Fig.10 Drain-Source Leakage Current vs. Junction Temperature**



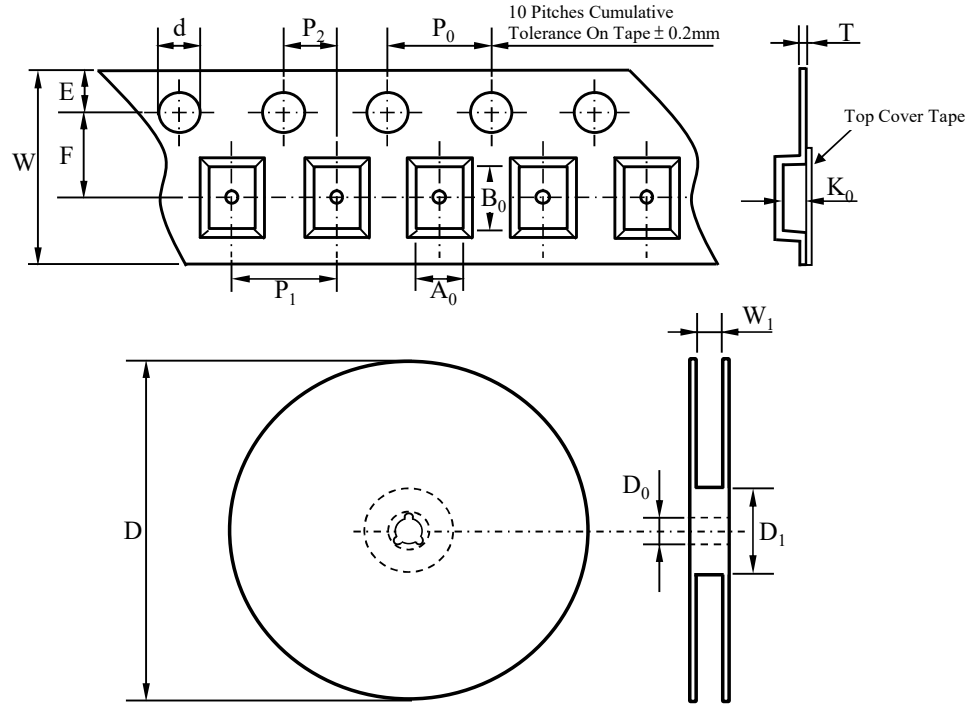
**Fig.11 Gate Charge Characteristics**



# SM03N650KLPH

## N-Channel Enhancement Mode Field Effect Transistor

### TAPE & REEL SPECIFICATION



Item	Symbol	DFN1006-3
Carrier width	$A_0$	*
Carrier length	$B_0$	
Carrier depth	$K_0$	
Sprocket hole	d	$1.50 \pm 0.10$
Reel outside diameter	D	$178.00 \pm 2.00$
Feed hole width	$D_0$	$13.00 \pm 0.50$
Reel inner diameter	$D_1$	MIN. 54.00
Sprocket hole position	E	$1.75 \pm 0.10$
Punch hole position	F	$3.50 \pm 0.10$
Sprocket hole pitch	$P_0$	$4.00 \pm 0.10$
Punch hole pitch	$P_1$	$2.00 \pm 0.10$
Embossment center	$P_2$	$2.00 \pm 0.10$
Overall tape thickness	T	MAX. 0.60
Tape width	W	$8.00 \pm 0.30$
Reel width	$W_1$	$8.40 \pm 1.50$

Note \*:  $A_0$ ,  $B_0$ , and  $K_0$  are determined by component size. The clearance between the components and the cavity must be within 0.05 mm min. to 0.5 mm max.

### ORDER INFORMATION

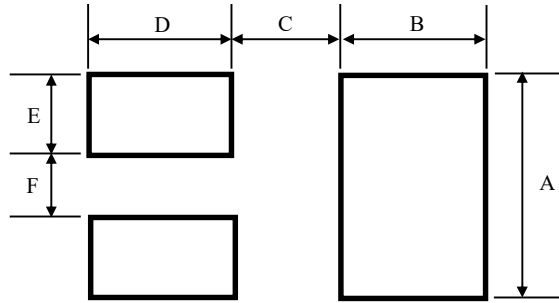
Part Number	Marking Code	Reel Size	Quantity
SM03N650KLPH	MS	7"	10,000



# SM03N650KLPH

*N-Channel Enhancement Mode Field Effect Transistor*

## **SUGGESTED SOLDER PAD LAYOUT**



Unit : mm

PACKAGE	A	B	C	D	E	F
DFN1006-3	0.60	0.40	0.30	0.40	0.25	0.20