



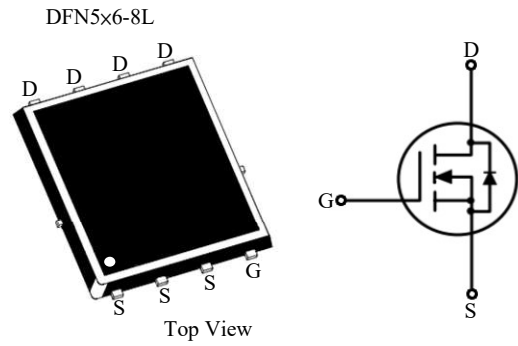
# SDM5E6N030LSX8H

## N-Channel Enhancement Mode Field Effect Transistor

### FEATURES

- Low  $R_{DS(on)}$
- Suffix "H" indicates Halogen-free parts, ex.SDM5E6N030LSX8H

### PIN CONFIGURATION



D	Drain
G	Gate
S	Source

### Maximum Ratings ( $T_A=25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	$V_{DS}$	65	V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$		
Continuous Drain Current	$I_D$	$T_C=25\text{ }^\circ\text{C}$	115.0	A
		$T_C=100\text{ }^\circ\text{C}$	72.5	
Pulsed Drain Current (Note 1)	$I_{DM}$	480	A	
Avalanche Current	$I_{AS}$	60.9	A	
Avalanche Energy (Note 2)	$E_{AS}$	185.4	mJ	
Power Dissipation	$P_D$	63.8	W	
Thermal Resistance from Junction to Ambient (Note 3)	$R_{\theta JA}$	39	$^\circ\text{C}/\text{W}$	
Thermal Resistance from Junction to Case	$R_{\theta JC}$	1.9	$^\circ\text{C}/\text{W}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	

Note:

1. The data tested by pulsed, pulse width  $\leq 100\mu\text{s}$ , duty cycle  $\leq 2\%$ , Reptitive rating, pulse width limited by junction temperature  $T_{J(MAX)}=150\text{ }^\circ\text{C}$ .
2. Limited by  $T_{J(MAX)}$ , starting  $T_J=25\text{ }^\circ\text{C}$ ,  $L=0.1\text{mH}$ ,  $R_g=25\Omega$ ,  $I_{AS}=60.9\text{A}$ ,  $V_{GS}=10\text{V}$ .
3. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch<sup>2</sup> copper plate in still air.



# SDM5E6N030LSX8H

## N-Channel Enhancement Mode Field Effect Transistor

### Electrical Characteristics ( $T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$	$V_{(BR)DSS}$	65	-	-	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(th)}$	1.2	-	2.5	V
Zero Gate Voltage Drain Current	$V_{DS} = 65\text{V}$	$I_{DSS}$	-	-	1	$\mu\text{A}$
Gate Leakage Current	$V_{GS} = \pm 20\text{V}$	$I_{GSS}$	-	-	$\pm 100$	nA
Drain-Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 30\text{A}$	$R_{DS(on)}$	-	2.4	3.0	m $\Omega$
	$V_{GS} = 4.5\text{V}, I_D = 20\text{A}$		-	-	4.5	
Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 20\text{A}$	$g_{FS}$	-	62.1	-	S
<b>Dynamic</b>						
Gate Resistance	$V_{DS} = 0\text{V}, V_{GS} = \text{V}, f = 1\text{MHz}$	$R_g$	-	1.2	-	$\Omega$
Total Gate Charge	$V_{DS} = 30\text{V}, V_{GS} = 4.5\text{V}, I_D = 30\text{A}$	$Q_g$	-	40.0	-	nC
			-	78.5	-	
Gate-Source Charge	$V_{DS} = 30\text{V}, V_{GS} = 10\text{V}, I_D = 30\text{A}$	$Q_{gs}$	-	13.0	-	nC
Gate-Drain Charge		$Q_{gd}$	-	18.0	-	
Input Capacitance	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	$C_{iss}$	-	4128	-	pF
Output Capacitance		$C_{oss}$	-	1245	-	
Reverse Transfer Capacitance		$C_{rss}$	-	34	-	
Turn on Delay Time		$t_{d(on)}$	-	26	-	
Turn on Rise Time	$V_{DS} = 30\text{V}, I_D = 30\text{A}$	$t_r$	-	44	-	
Turn off Delay Time		$V_{GS} = 10\text{V}, R_g = 3.3\Omega$	$t_{d(off)}$	-	25	-
Turn off Fall Time	$t_f$		-	6	-	
<b>Drain-Source Body Diode</b>						
Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1\text{A}$	$V_{SD}$	-	-	1.3	V
Diode Continuous Forward Current	-	$I_S$	-	-	115	A
Diode Pulse Current		$I_{SM}$	-	-	480	A
Reverse Recovery Time	$I_S = 30\text{A}, di/dt = 100\text{A}/\mu\text{s}$	$t_{rr}$	-	40	-	ns
Reverse Recovery Charge		$Q_{rr}$	-	33	-	nC



# SDM5E6N030LSX8H

## N-Channel Enhancement Mode Field Transistor

### RATINGS AND CHARACTERISTIC CURVES

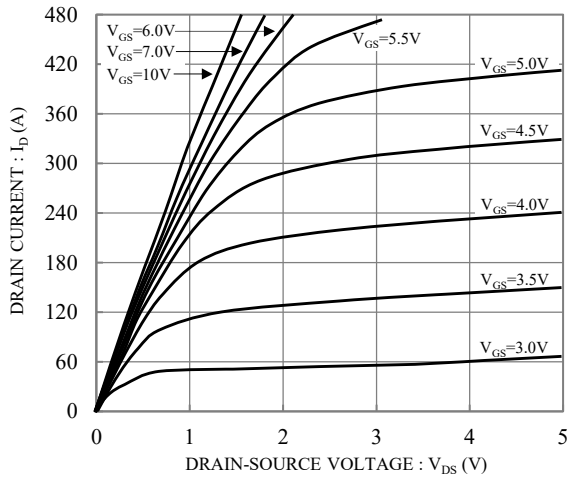


Fig.1 Typical Output Characteristics

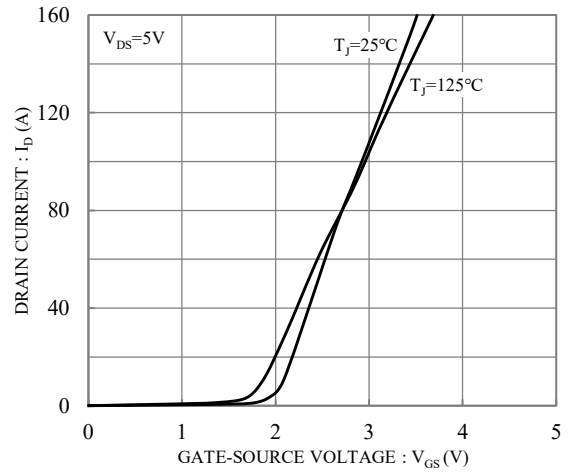


Fig.2 Typical Transfer Characteristics

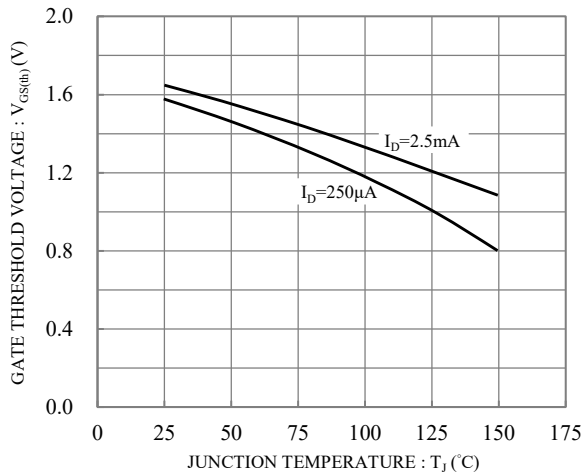


Fig.3 Gate Threshold Voltage vs. Junction Temperature

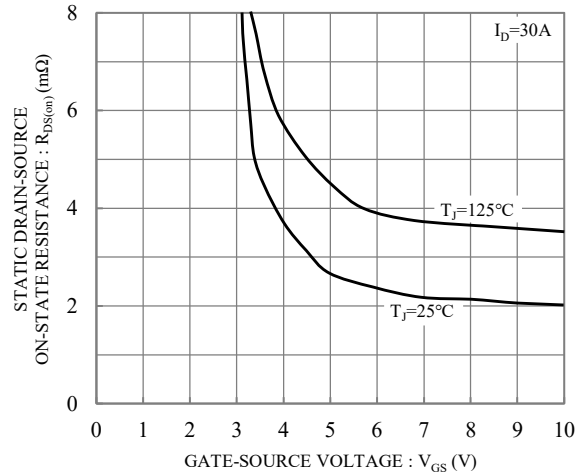


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

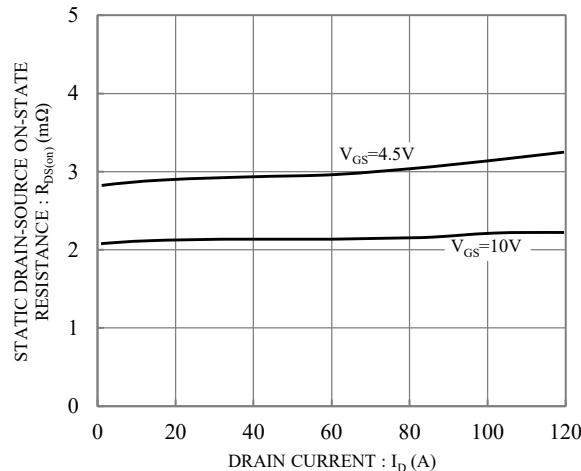


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

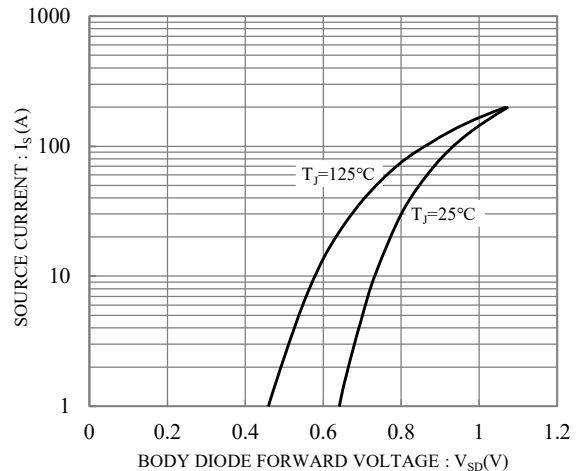
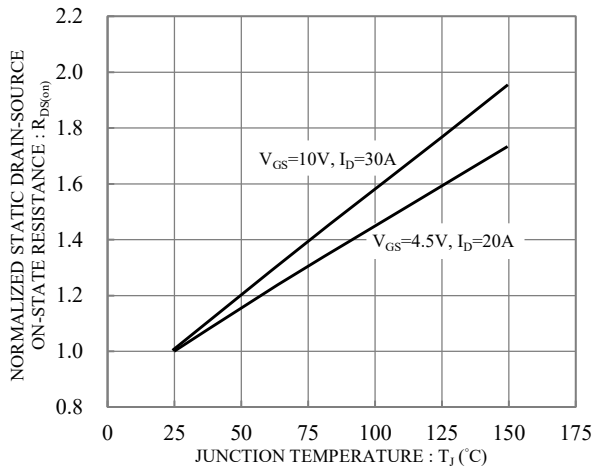


Fig.6 Body Diode Forward Voltage vs. Source Current

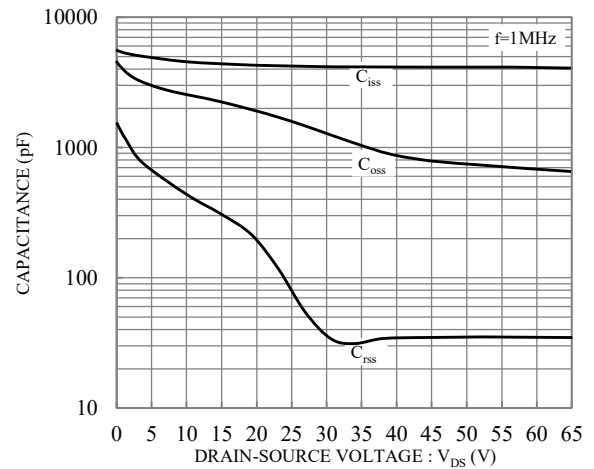


# SDM5E6N030LSX8H

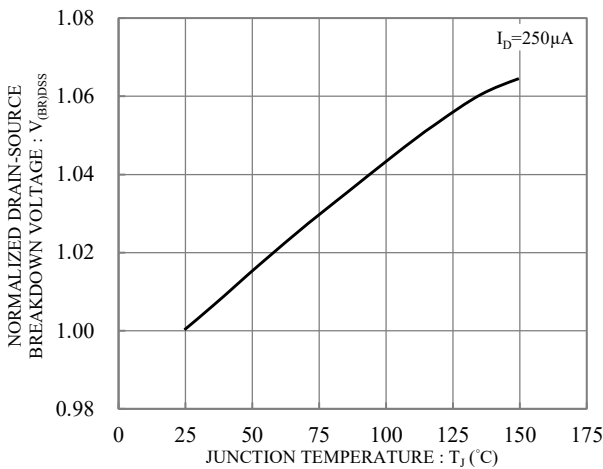
## N-Channel Enhancement Mode Field Effect Transistor



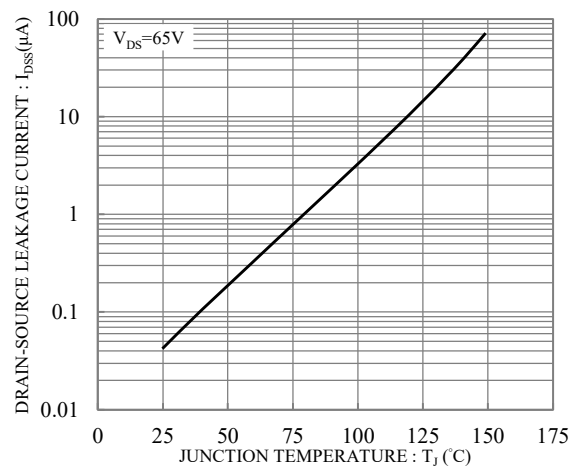
**Fig.7 Drain-Source On-State Resistance vs. Junction Temperature**



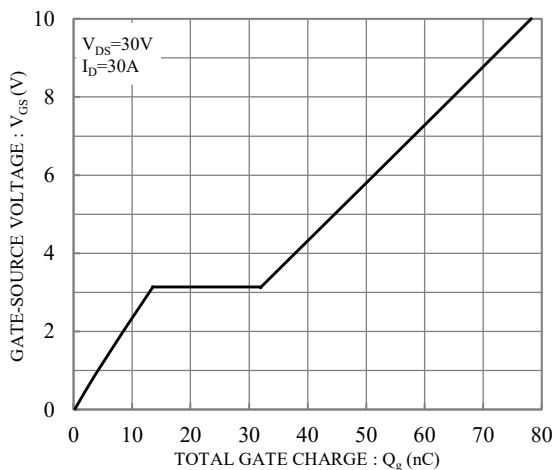
**Fig.8 Capacitance vs. Drain-Source Voltage**



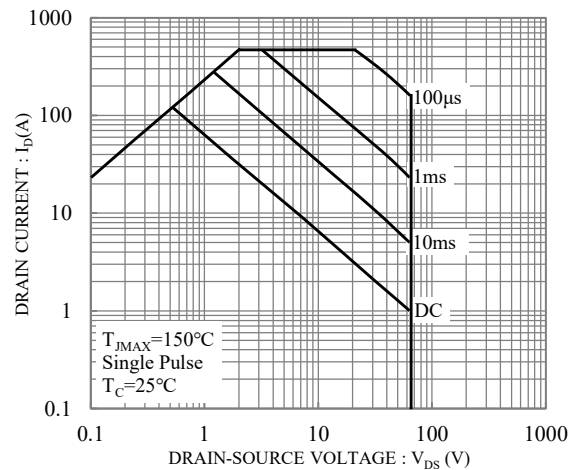
**Fig.9 Breakdown Voltage vs. Junction Temperature**



**Fig.10 Drain-Source Leakage Current vs. Junction Temperature**



**Fig.11 Gate Charge Characteristics**



**Fig.12 Safe Operation Area**



# SDM5E6N030LSX8H

## N-Channel Enhancement Mode Field Effect Transistor

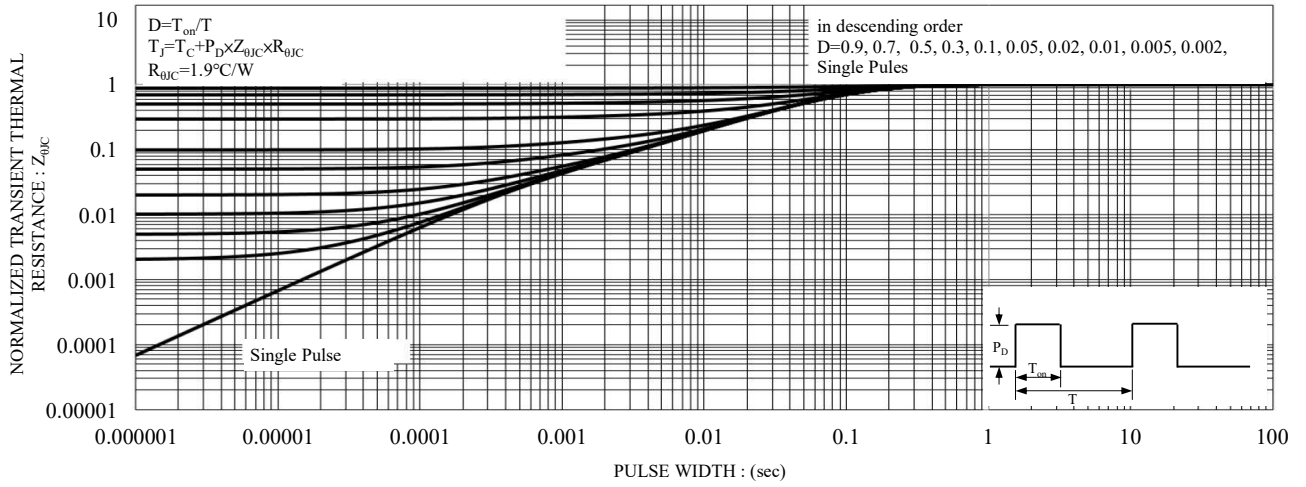


Fig.13 Maximum Transient Thermal Impedance

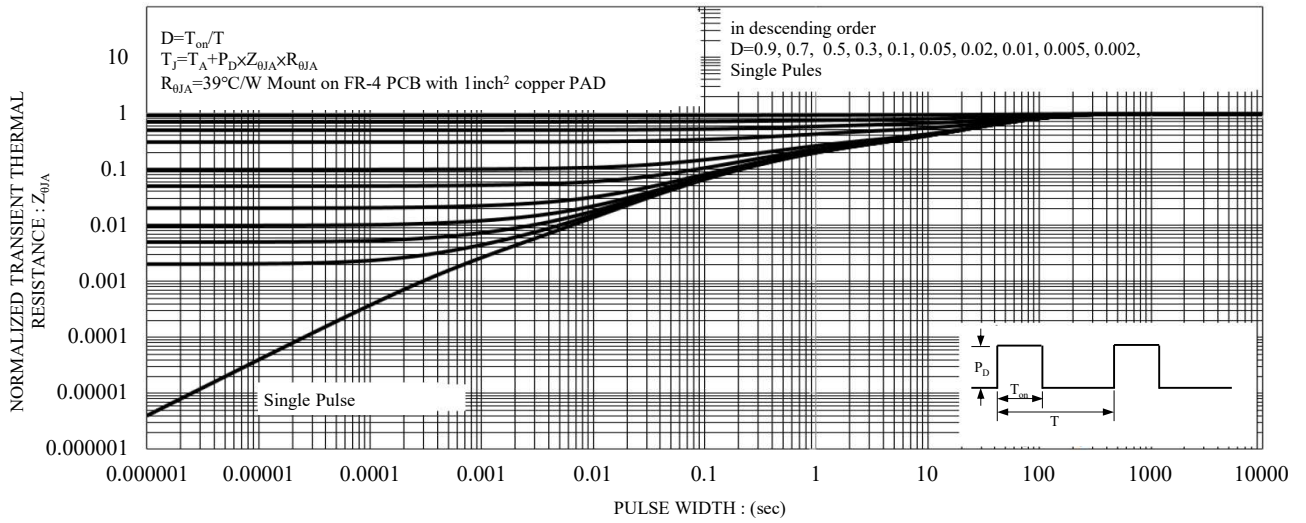


Fig.14 Maximum Transient Thermal Impedance

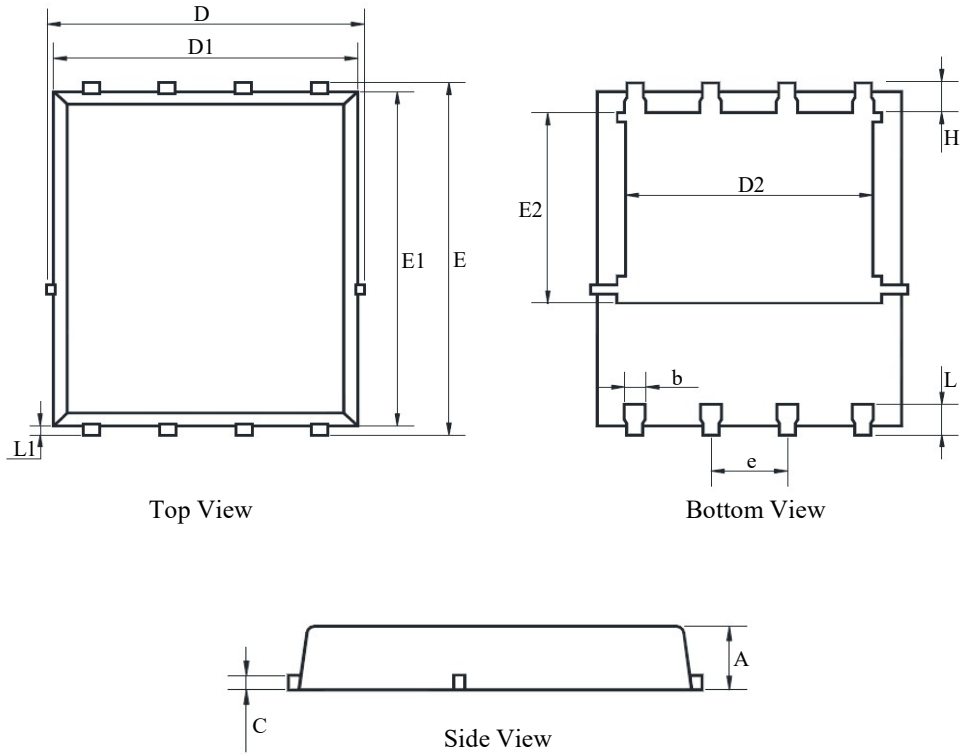


# SDM5E6N030LSX8H

## N-Channel Enhancement Mode Field Effect Transistor

### PACKAGE DIMENSION

#### DFN5×6-8L



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.12	0.035	0.044
b	0.33	0.51	0.013	0.020
C	0.11	0.34	0.004	0.013
D	4.70	5.26	0.185	0.207
D1	4.70	5.10	0.185	0.201
D2	3.56	4.50	0.140	0.177
E	5.75	6.25	0.226	0.246
E1	5.60	6.00	0.220	0.236
E2	3.18	3.66	0.125	0.144
e	1.17	1.37	0.046	0.054
L	0.35	0.71	0.014	0.028
L1	0.06	0.20	0.002	0.008
H	0.35	0.71	0.014	0.028