



ASDM610N170LSX8H

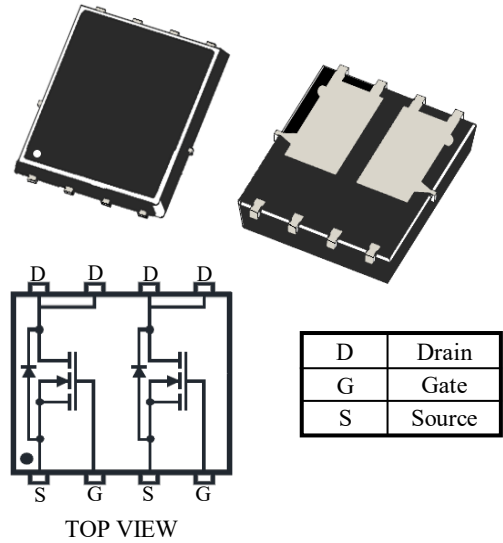
Dual N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- Low $R_{DS(on)}$
- AEC-Q101 Qualified
- Suffix "H" indicates Halogen-free parts, ex. ASDM610N170LSX8H

PIN CONFIGURATION

DFN5x6-8L



Maximum Ratings ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	V_{DS}	100	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	I_D	$T_C=25^\circ\text{C}$	34	A
		$T_C=100^\circ\text{C}$	21	
Pulsed Drain Current (Note 1)	I_{DM}	130	A	
Avalanche Current	I_{AS}	17.4	A	
Single Pulse Avalanche Energy (Note 2)	E_{AS}	15	mJ	
Power Dissipation	P_D	32.7	W	
Thermal Resistance from Junction to Ambient (Note 3)	$R_{\theta JA}$	80	$^\circ\text{C}/\text{W}$	
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3.8	$^\circ\text{C}/\text{W}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	

- Note:
1. The data tested by pulsed, pulse width $\leq 100\mu\text{s}$, duty cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}=150^\circ\text{C}$.
 2. Limited by $T_{J(MAX)}$, starting $T_J=25^\circ\text{C}$, $L=0.1\text{mH}$, $R_g=25\Omega$, $I_{AS}=17.4\text{A}$, $V_{GS}=10\text{V}$.
 3. Device mounted on FR-4 substrate PC board, 2oz copper, with 1 inch² copper plate in still air.



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Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$I_D = 250\mu\text{A}$	$V_{(BR)DSS}$	100	-	-	V	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	$V_{GS(th)}$	1.2	-	2.5	V	
Zero Gate Voltage Drain Current	$V_{DS} = 80\text{V}$	I_{DSS}	-	-	1	μA	
Gate Leakage Current	$V_{GS} = \pm 20\text{V}$	I_{GSS}	-	-	± 100	nA	
Drain-Source On-Resistance	$V_{GS} = 10\text{V}, I_D = 7\text{A}$	$R_{DS(on)}$	-	15	21	m Ω	
	$V_{GS} = 4.5\text{V}, I_D = 5\text{A}$		-	-	26		
Dynamic							
Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 7\text{A}$	g_{FS}	-	15.8	-	S	
Gate Resistance	$V_{DS} = 0\text{V}, f = 1\text{MHz}$	R_g	-	0.6	-	Ω	
Total Gate Charge	$V_{DS} = 50\text{V}, V_{GS} = 4.5\text{V}, I_D = 7\text{A}$	Q_g	-	12	-	nC	
			-	22	-		
Gate-Source Charge	$V_{DS} = 50\text{V}, V_{GS} = 10\text{V}, I_D = 7\text{A}$	Q_{gs}	-	4	-		
Gate-Drain Charge		Q_{gd}	-	6	-		
Input Capacitance	$V_{DS} = 50\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	C_{iss}	-	1028	-	pF	
Output Capacitance		C_{oss}	-	170	-		
Reverse Transfer Capacitance		C_{rss}	-	7	-		
Turn on Delay Time		$V_{DS} = 50\text{V}, I_D = 7\text{A}$	$t_{d(on)}$	-	12.0	-	ns
Turn on Rise Time	t_r		-	3.5	-		
Turn off Delay Time	$V_{GS} = 10\text{V}, R_g = 4.7\Omega$		$t_{d(off)}$	-	11.0	-	
Turn off Fall Time			t_f	-	4.0	-	
Drain-Source Body Diode							
Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 1\text{A}$	V_{SD}	-	-	1.2	V	
Diode Continuous Forward Current	-	I_S	-	-	34	A	
Diode Pulse Current		I_{SM}	-	-	130	A	
Reverse Recovery Time	$I_S = 7\text{A}, di/dt = 100\text{A}/\mu\text{s}$	t_{rr}	-	40	-	ns	
Reverse Recovery Charge		Q_{rr}	-	30	-	nC	



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RATINGS AND CHARACTERISTIC CURVES

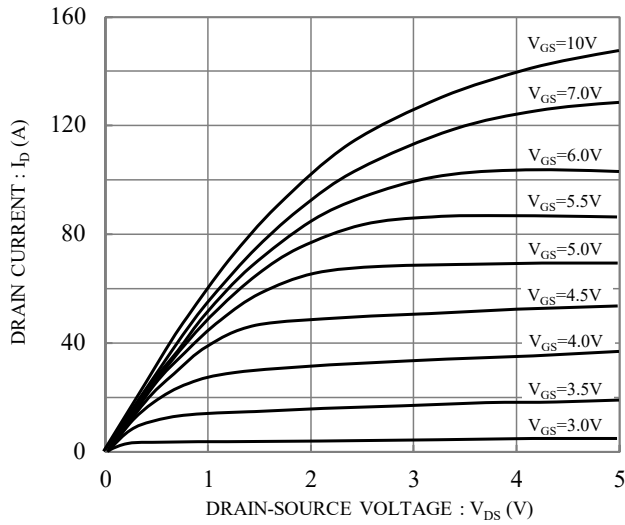


Fig.1 Typical Output Characteristics

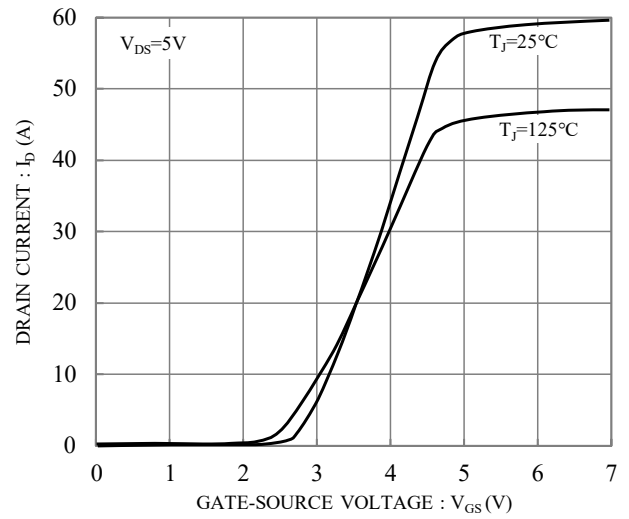


Fig.2 Typical Transfer Characteristics

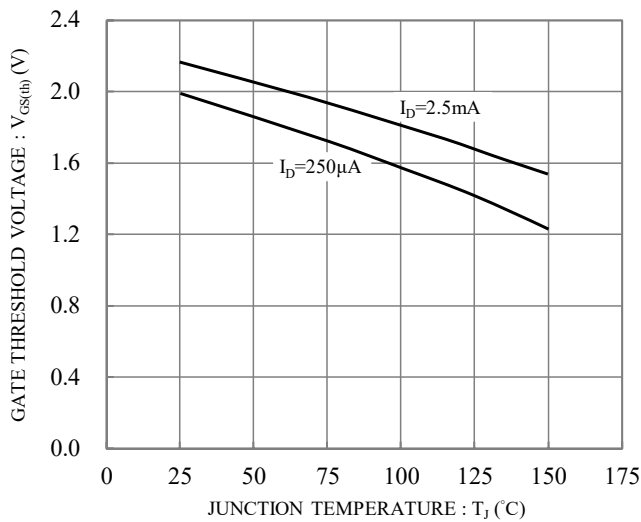


Fig.3 Gate Threshold Voltage vs. Junction Temperature

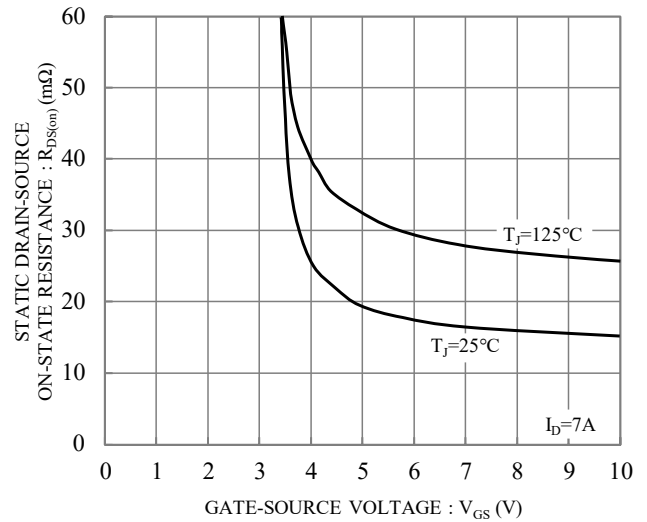


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

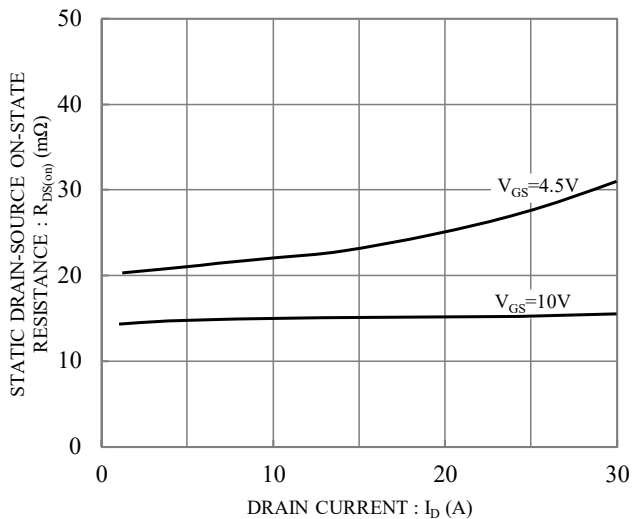


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

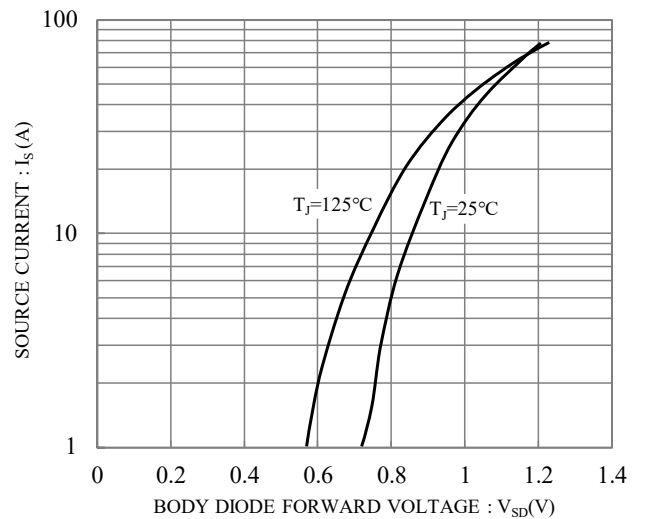


Fig.6 Body Diode Forward Voltage vs. Source Current



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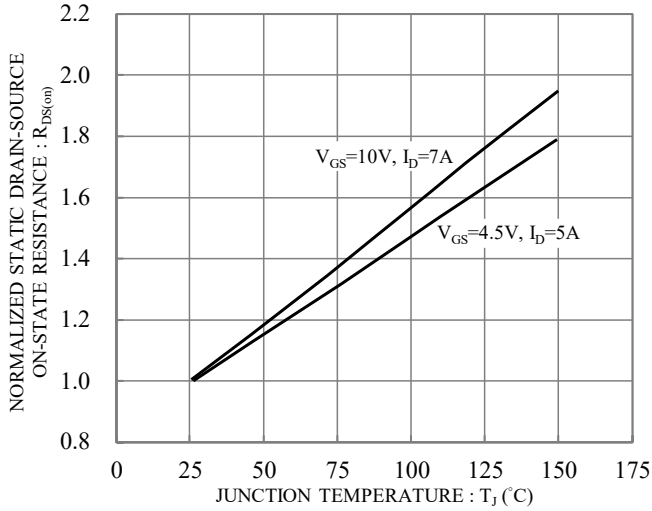


Fig.7 Drain-Source On-State Resistance vs Junction Temperature

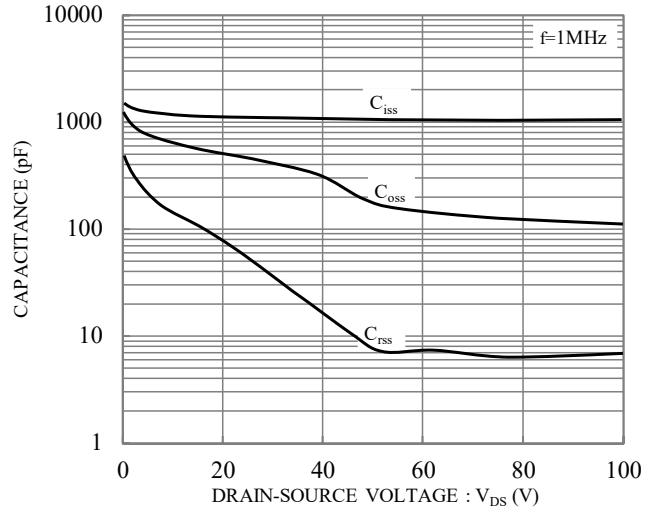


Fig.8 Capacitance vs Drain-Source Voltage

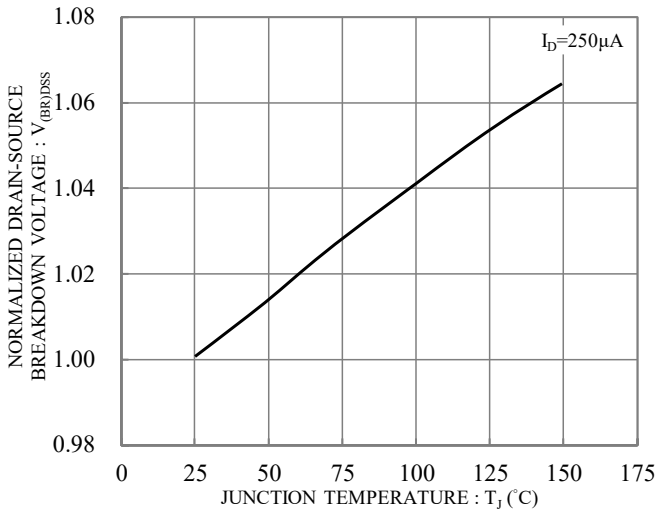


Fig.9 Breakdown Voltage vs Junction Temperature

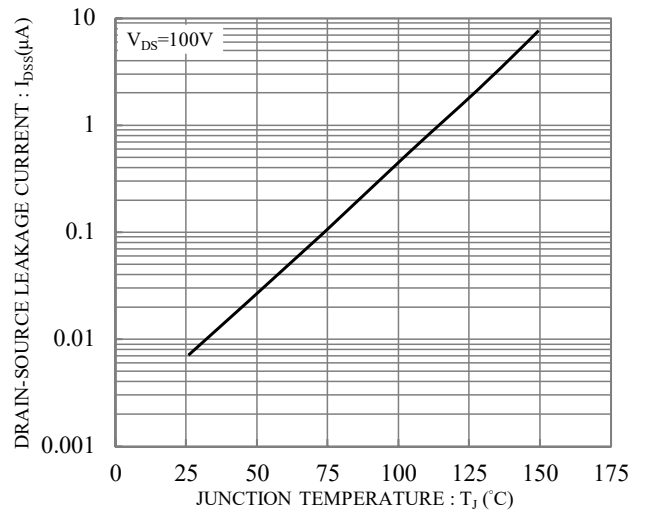


Fig.10 Drain-Source Leakage Current vs Junction Temperature

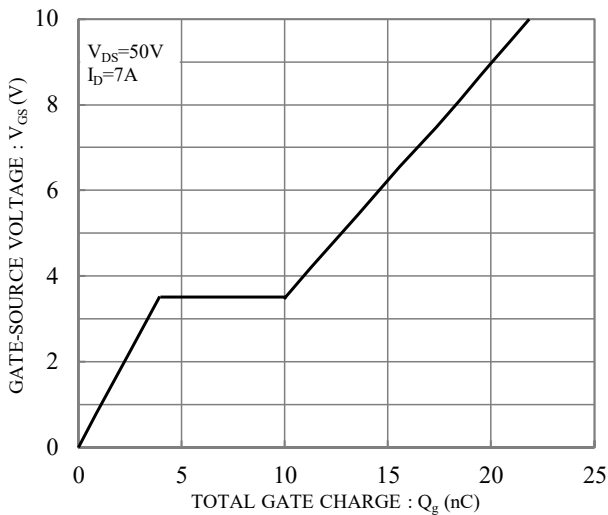


Fig.11 Gate Charge Characteristics

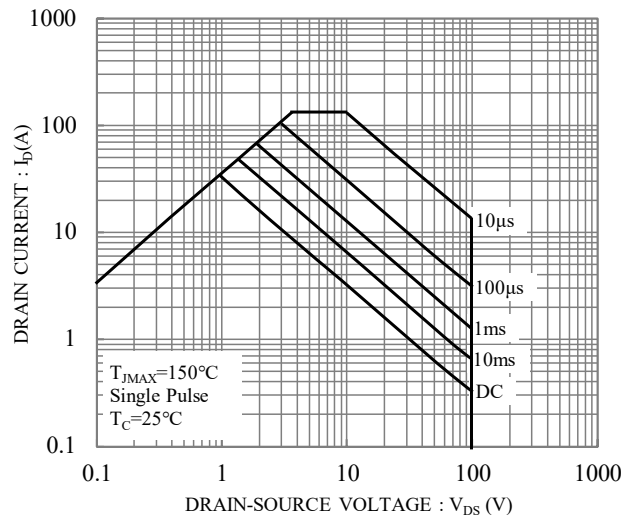


Fig.12 Safe Operation Area



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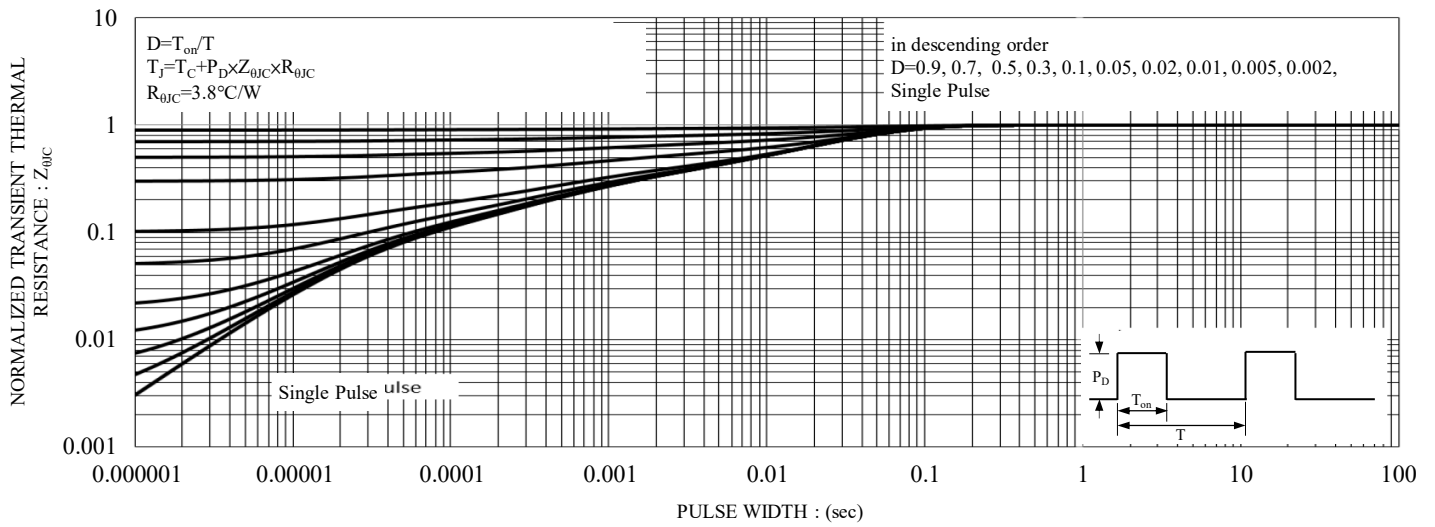


Fig.13 Maximum Transient Thermal Impedance

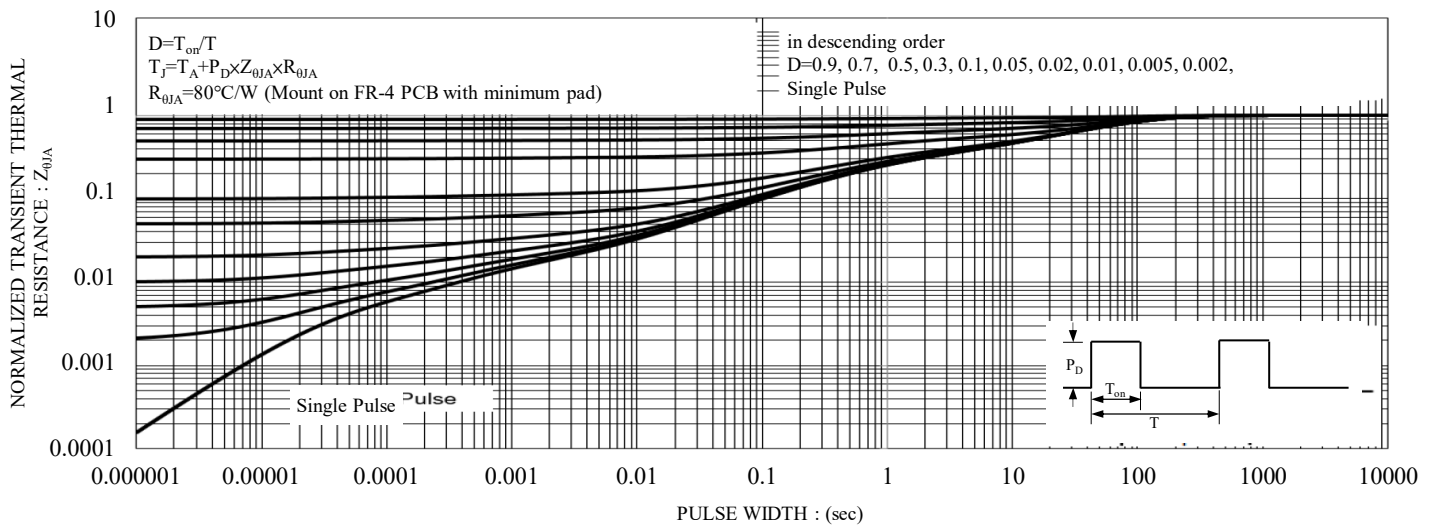


Fig.14 Maximum Transient Thermal Impedance

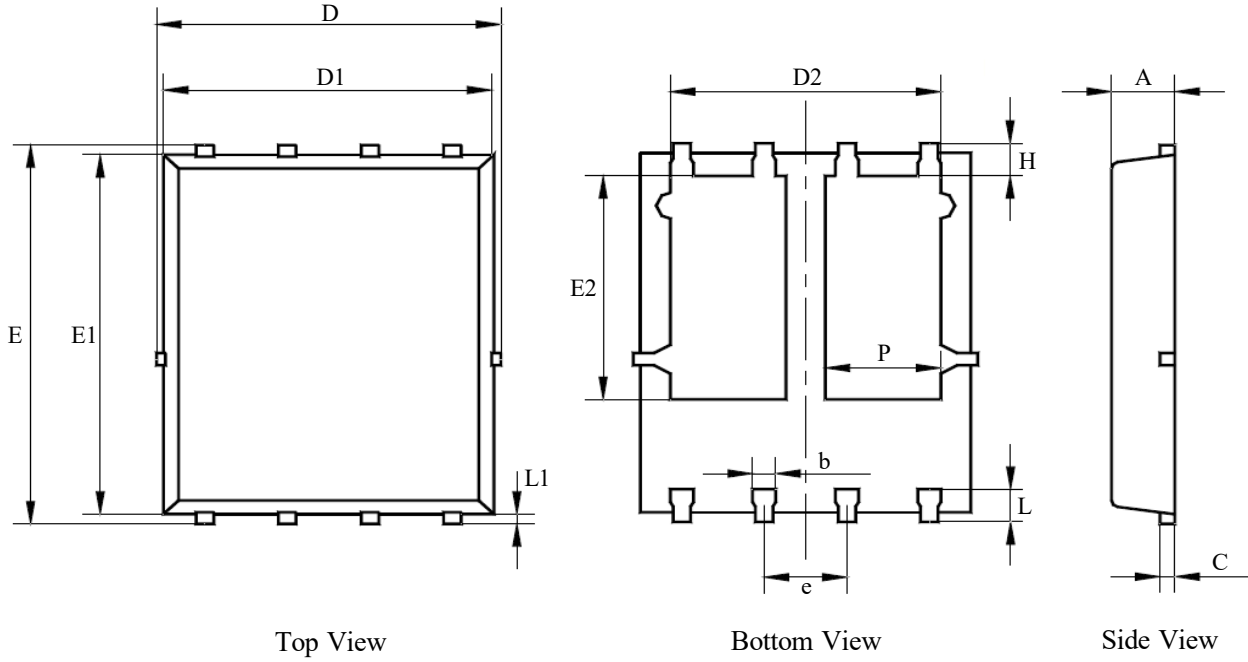


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PACKAGE DIMENSION

DFN5×6-8L



Top View

Bottom View

Side View

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.90	1.12	0.035	0.044
b	0.33	0.51	0.013	0.020
C	0.11	0.34	0.004	0.013
D	4.70	5.26	0.185	0.207
D1	4.70	5.10	0.185	0.201
D2	3.56	4.50	0.140	0.177
E	5.75	6.25	0.226	0.246
E1	5.60	6.00	0.220	0.236
E2	3.18	3.66	0.125	0.144
e	1.17	1.37	0.046	0.054
L	0.35	0.71	0.014	0.028
L1	0.06	0.20	0.002	0.008
H	0.35	0.71	0.014	0.028
P	1.70	2.30	0.067	0.091



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SUGGESTED SOLDER PAD LAYOUT

