



ASDM3E6N085LSH8H

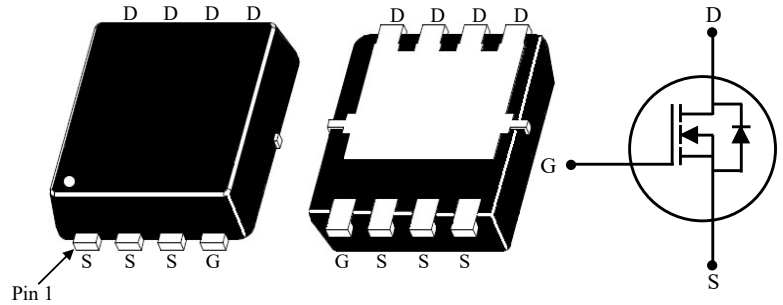
N-Channel Enhancement Mode Field Effect Transistor

FEATURES

- AEC-Q101 Qualified
- Suffix "H" indicates Halogen-free parts, ex.ASDM3E6N085LSH8H.

PIN CONFIGURATION

DFN3x3-8L



D	Drain
G	Gate
S	Source

Maximum Ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-Source Voltage	V_{DS}	65	V	
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current	I_D	$T_C = 25^\circ\text{C}$	48	A
		$T_C = 100^\circ\text{C}$	30	
Pulsed Drain Current (Note 1)	I_{DM}	160	A	
Avalanche Current	I_{AS}	12	A	
Avalanche Energy (Note 2)	E_{AS}	36	mJ	
Power Dissipation	P_D	41.7	W	
Thermal Resistance from Junction to Ambient (Note 3)	$R_{\theta JA}$	50	$^\circ\text{C}/\text{W}$	
Thermal Resistance from Junction to Case	$R_{\theta JC}$	3	$^\circ\text{C}/\text{W}$	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	

Note:

1. The data tested by pulsed, pulse width $\leq 100\mu\text{s}$, duty cycle $\leq 2\%$, Repetitive rating, pulse width limited by junction temperature $T_{J(\text{MAX})} = 150^\circ\text{C}$.
2. Limited by $T_{J(\text{MAX})}$, starting $T_J = 25^\circ\text{C}$, $L = 0.5\text{mH}$, $R_g = 25\Omega$, $I_{AS} = 12\text{A}$, $V_{GS} = 10\text{V}$.
3. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch² copper plate in still air.



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Electrical Characteristics ($T_A=25\text{ }^\circ\text{C}$ unless otherwise specified)

Parameter	Conditions	Symbol	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	$I_D=250\mu\text{A}$	$V_{(BR)DSS}$	65	-	-	V
Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	$V_{GS(th)}$	1.2	-	2.5	V
Zero Gate Voltage Drain Current	$V_{DS}=52\text{V}$	I_{DSS}	-	-	1	μA
Gate Leakage Current	$V_{GS}=\pm 20\text{V}$	I_{GSS}	-	-	± 100	nA
Drain-Source On-Resistance	$V_{GS}=10\text{V}, I_D=10\text{A}$	$R_{DS(on)}$	-	7.5	8.5	m Ω
	$V_{GS}=4.5\text{V}, I_D=8\text{A}$		-	12.0	16.0	
Forward Transconductance	$V_{DS}=5\text{V}, I_D=5\text{A}$	g_{FS}	-	13	-	S
Dynamic						
Gate Resistance	$V_{DS}=0\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	R_g	-	2	-	Ω
Total Gate Charge	$V_{DS}=30\text{V}, V_{GS}=4.5\text{V}, I_D=10\text{A}$	Q_g	-	7.2	-	nC
Gate-Source Charge			$V_{DS}=30\text{V}, V_{GS}=10\text{V}, I_D=10\text{A}$	Q_{gs}	-	
Gate-Drain Charge	$V_{DS}=30\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	Q_{gd}	-	2.6	-	pF
Input Capacitance		C_{iss}	-	2.8	-	
Output Capacitance	$V_{DS}=30\text{V}, V_{GS}=0\text{V}, f=1\text{MHz}$	C_{oss}	-	825	-	pF
Reverse Transfer Capacitance		C_{rss}	-	290	-	
Turn on Delay Time	$V_{DS}=30\text{V}, I_D=10\text{A}$ $V_{GS}=10\text{V}, R_g=4.7\Omega$	$t_{d(on)}$	-	15	-	ns
Turn on Rise Time		t_r	-	10	-	
Turn off Delay Time		$t_{d(off)}$	-	9	-	
Turn off Fall Time		t_f	-	2	-	
Drain-Source Body Diode						
Diode Forward Voltage	$V_{GS}=0\text{V}, I_S=1\text{A}$	V_{SD}	-	-	1.2	V
Diode Continuous Forward Current	-	I_S	-	-	48	A
Diode Pulse Current		I_{SM}	-	-	160	A
Reverse Recovery Time	$I_S=10\text{A}, di/dt=100\text{A}/\mu\text{s}$	t_{rr}	-	17	-	ns
Reverse Recovery Charge		Q_{rr}	-	6.5	-	nC



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RATINGS AND CHARACTERISTIC CURVES

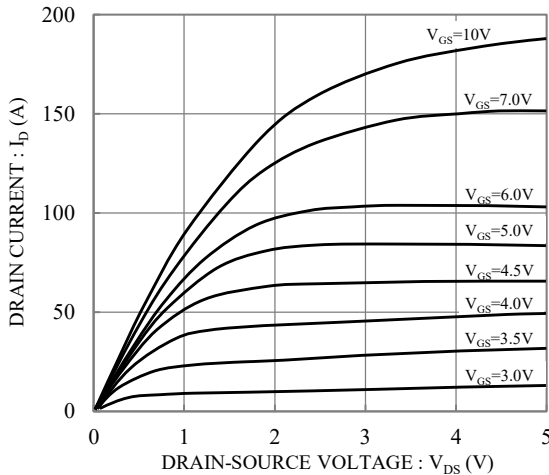


Fig.1 Typical Output Characteristics

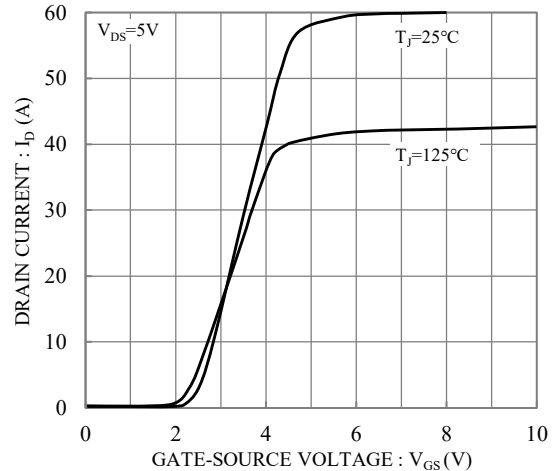


Fig.2 Typical Transfer Characteristics

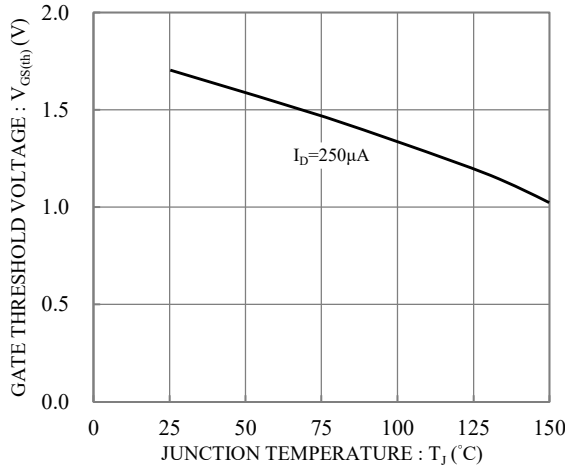


Fig.3 Gate Threshold Voltage vs. Junction Temperature

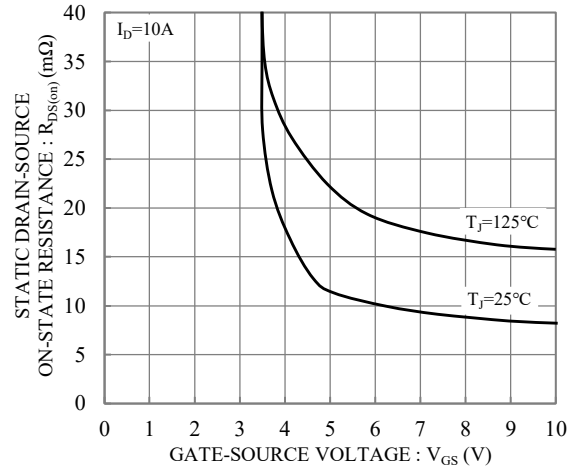


Fig.4 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

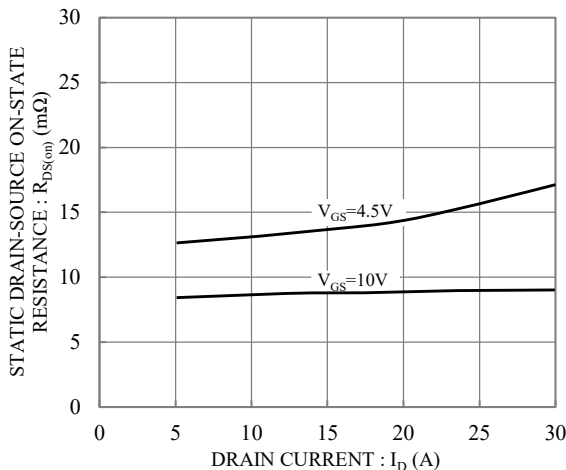


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current

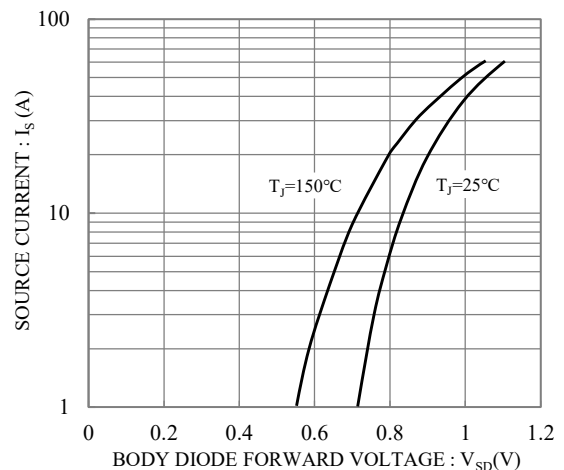


Fig.6 Body Diode Forward Voltage vs. Source Current



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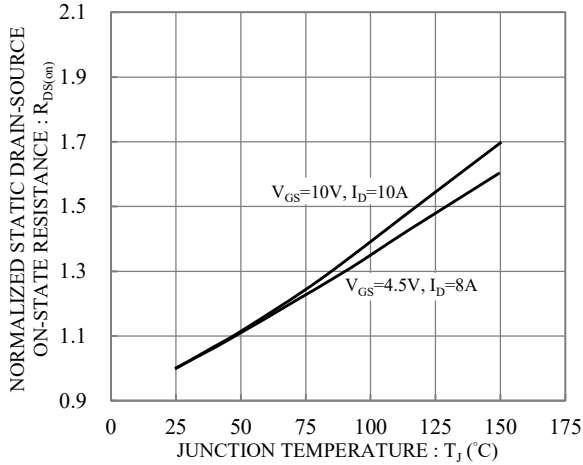


Fig.7 Drain-Source On-State Resistance vs. Junction Temperature

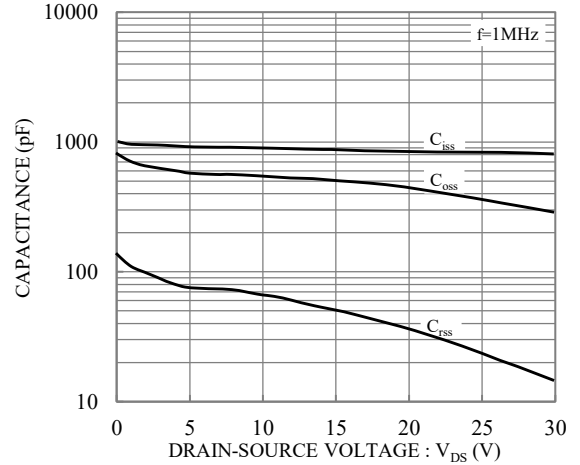


Fig.8 Capacitance vs. Drain-Source Voltage

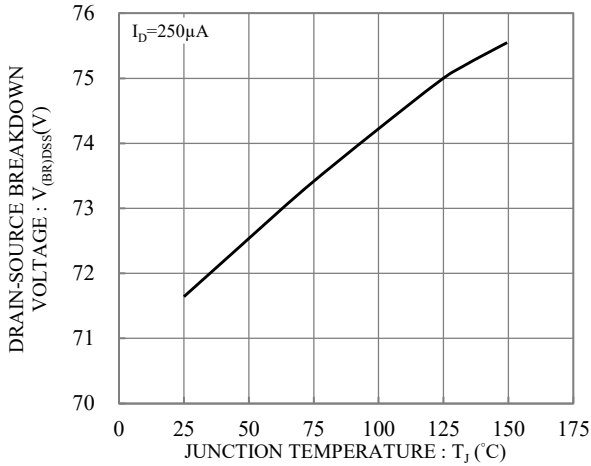


Fig.9 Breakdown Voltage vs. Junction Temperature

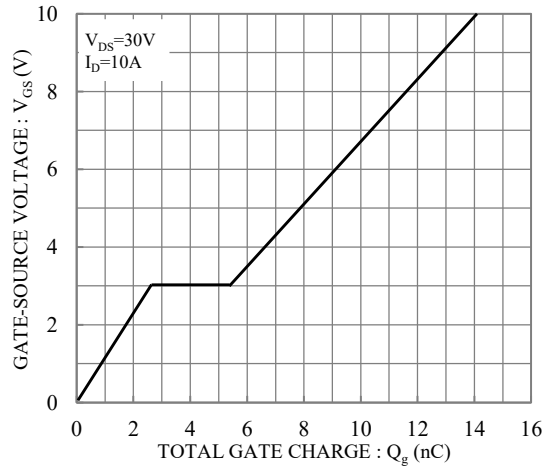


Fig.10 Gate Charge Characteristics

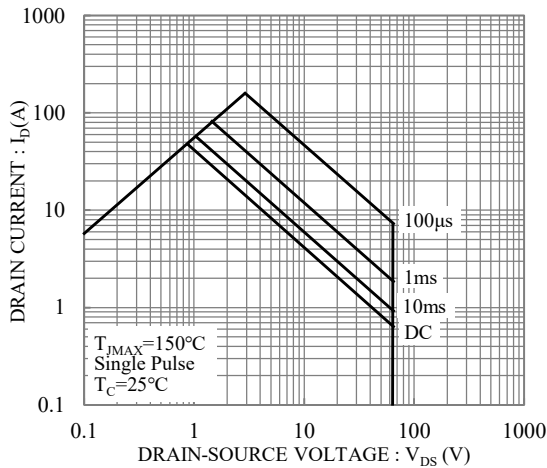


Fig.11 Drain-Source Leakage Current vs. Junction Temperature



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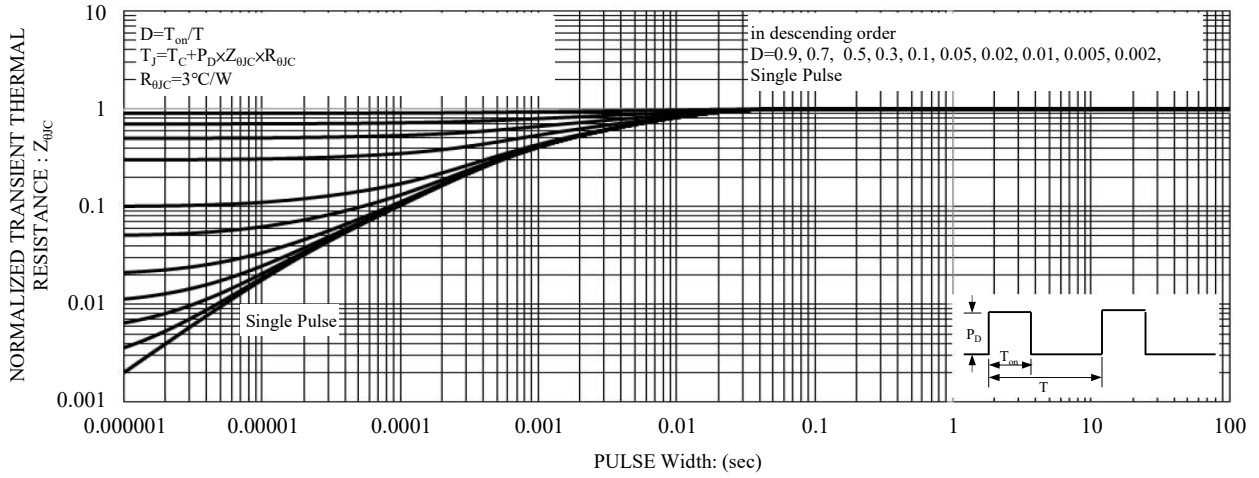


Fig.13 Maximum Transient Thermal Impedance

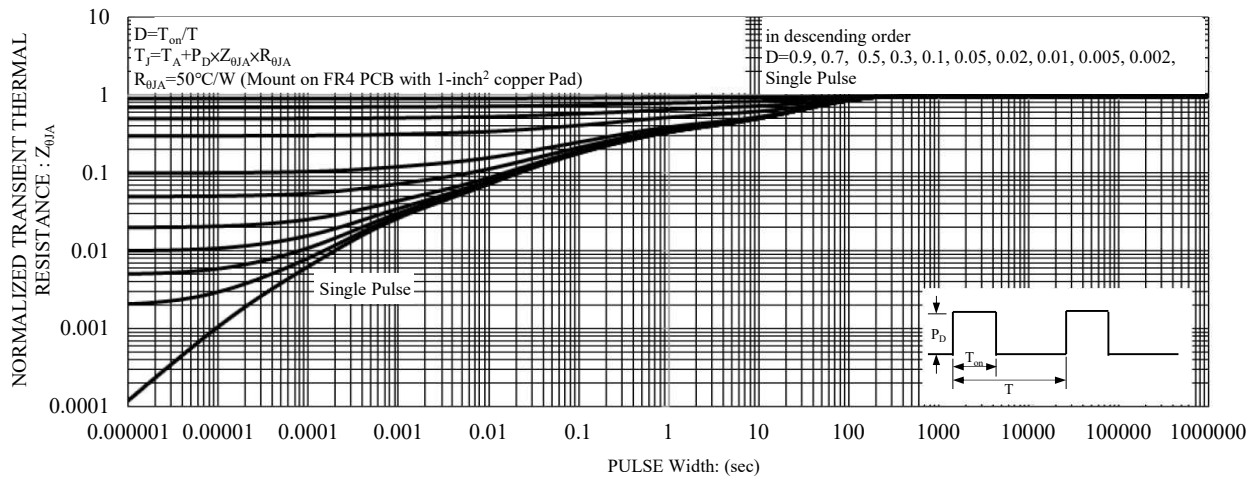


Fig.14 Maximum Transient Thermal Impedance

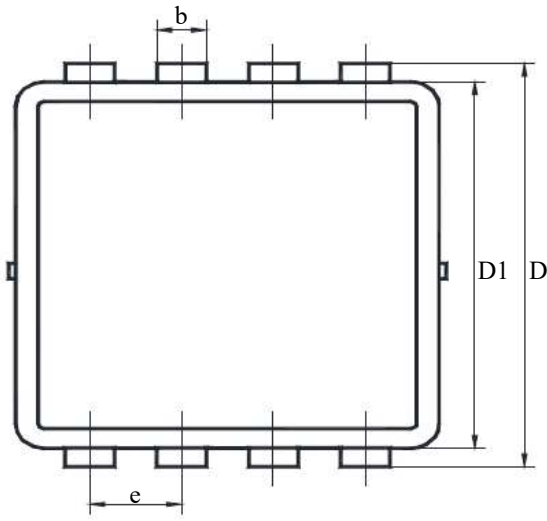


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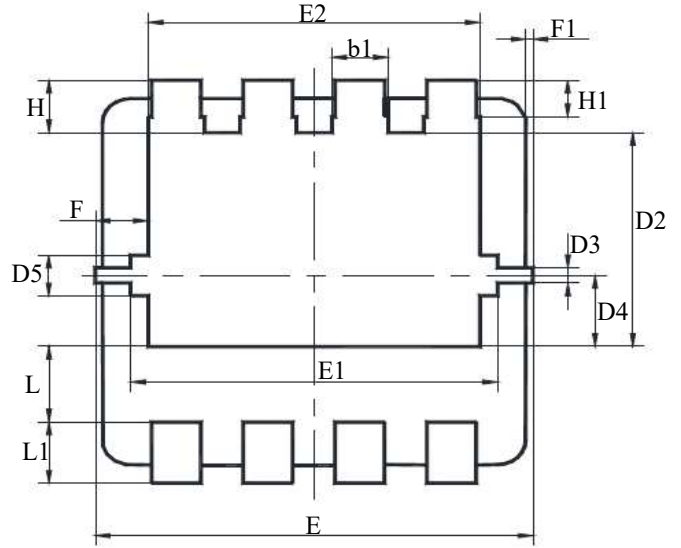
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PACKAGE DIMENSION

DFN3x3-8L



Top View



Bottom View



Side View

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	0.700	0.900	0.028	0.035
A1	0.100	0.250	0.004	0.010
A2	0.000	0.050	0.000	0.002
b	0.240	0.350	0.009	0.014
b1	0.300	0.500	0.012	0.020
D	3.100	3.300	0.122	0.130
D1	2.900	3.100	0.114	0.122
D2	1.650	1.850	0.065	0.073
D3	0.150	0.250	0.006	0.010
D4	0.480	0.680	0.019	0.027
D5	0.230	0.430	0.009	0.017
E	3.000	3.200	0.118	0.126
E1	2.500	2.700	0.098	0.106
E2	2.400	2.600	0.094	0.102
e	0.600	0.700	0.024	0.028
F	0.275	0.475	0.011	0.019
F1	0.000	0.100	0.000	0.004
L	0.520	0.720	0.020	0.028
L1	0.300	0.500	0.012	0.020
H	0.330	0.530	0.013	0.021
H1	0.200	0.400	0.008	0.016



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SUGGESTED SOLDER PAD LAYOUT

